THE INTERAK FDC-1 CARD

The FDC-1 card is one of the most complicated cards in the Interak computer. It is a measure of how advanced it is, and confirmation of the strength of the basic structure of Interak, that while the FDC-1 could not have been built when these cards were first designed, it yet can be easily fitted into an Interak system.

Of course according to Interak principles, the use of the major chip in this design the FDC (Floppy Disk Controller) chip itself should be prohibited. As far as possible, only standard readily understood parts such as gates latches and flip-flops should be used in an Interak design. These laudable aims are impractical in the case of a sub system as complex as a floppy disk controller; literally hundreds of simple logic packages would be required and would be an absolute nightmare to design build and set up. (By the same argument, although it is possible to build a Z80-CPU chip out of ordinary logic functions, and some brave souls have actually done it, the majority of us can see the sense in simply purchasing such an item ready made. There is no fundamental betrayal of our high principles here; we are still building a finished system from its individual parts, all that has happened is that it is a more powerful system than we ever thought it would be when it began, and it therefore has to use more powerful building blocks.)

In Praise of the 2797 FDC Chip

It is quite easy to design a floppy disk interface, but not so easy to get it right. Proof of this is to be had by the examination of a good 50% or more of commercial ready made computers (of the "home computer" genus particularly). Granted, they have sold countless hundreds of thousands, but they often have the most glaring flaws in their design. Granted, there are probably flaws in our design, but a lot of work has been done (and here the assistance of our very talented and enthusiastic users is gratefully acknowledged) to make sure that there remain none we know of. Typical of the weaker "home computer" designs are faults which make for poor reliability. Such nonsense is heard as only one or two makes of drive can be used, or the drives can be expected to lose data if they have been abused by being used all morning, only certain makes of diskette will do, and so on. This is like saying the design of a motor car is such that it will only run on a few particular makes of petrol. No doubt there are differences in brands of petrol; no doubt some may be better than other, but a motorist has a right to expect his car to perform reliably whatever make of petrol he uses (within reason). Those of us who have been brought up on computers with poor tape systems, will have been through this - searching for that particular brand of tape, the only one which will give the magic results, and then been amazed at how reliable tape can be with almost any old tape once a properly designed system (such as Interak?) has been built.

But what has this to do with the choice of FDC chip? The 2797 represents the answer to all our prayers. It has all the frills which are so essential to reliability (phase locked loop, automatic write enable precompensation etc.) which are so hard to design (properly) without great experience, and they have been built into the chip, by experts.

The 2797 was designed by the Western Digital company of America, who are specialists in the field. It is so good that the design has been adopted by Texas Instruments too. Texas Instruments of course make their own FDC chips (lots of them) but it is significant that they have been able to see the merits of a competitor's product.

The beauty of the 2797 from the constructor's point of view is that, because of the large scale integration, the very best methods of writing and reading data on a floppy disk have been incorporated. When such items as the phase locked loop and the data separator were separate chips outside the main FDC chip, the designer (again "home computers" particularly) was under tremendous pressure to save a few pounds by leaving them out if he could, and using simpler methods. Look inside the average home computer and you will see no phase locked loop for this purpose. Don't make the mistake of assuming that it then must be inside the FDC chip: unless it is one of the 2797 series, it probably isn't - it's been left out for cheapness, or perhaps through lack of knowledge. Maybe the prototype worked fine with its brand new disks and drives, without all this complexity, but what about later when a bit of tolerance is needed, how well did it work for the user, once the three months' guarantee was up? Who cares? You and I do for a start!

So, more concisely; the 2797 is the very best chip we can use. It is designed by experts, supported too by a mighty semiconductor manufacturer, and yet as easy as can be to set up and use (all the clever stuff goes on inside the chip). I think it is a winner.

The FDC-1 Card Design

One glance at the parts list reaveals that for a "single chip" controller, the 2797 seems to need a lot of help! Suffice it to say that none of the extra support components have been added lightly. This board has been several years in development and many of these extras have been added to satisfy some particular need of those who have been setting up special systems for special purposes. Although in a floppy disk system the hardware is only the half of it (the disk operating system ~~hard~~soft ware is the other half, or more!) there is nothing in the design of the hardware to prevent any known type of disk drive of any diameter to be used, in virtually any permutation. (As hinted at, the software is another matter, but all it needs for esoteric system software is for someone to write it.) Up to 4 drives, of all manners of formats, densities, number of sides, diameters etc. can be accommodated by one FDC-1 card, and sufficient address decoding has been provided to allow up to 32 such cards to be fitted (although for other reasons this is a impractical and utterly fanciful idea).

To allow for this great flexibility has presented a dilemma to the board's designers. Should the board be made impossible to build and easy to use, or should it be made easy to build and imossible to use? Rather than solve that dilemma another approach was used. All of the multifarious options have been made selectable, by switches, DIL headers, and push fit "Jumper" Links. In its standard form, the kit of parts includes everything you need to do everything. There is no need to know at the time of construction exactly how the board is to be set up for its

ultimate use, these are all options which it is easy to select and alter later, as far as possible without the use of a soldering iron. Be honest, would you know now at this stage if you will use the "motors on" monostable with a 5 second delay or a 10 second delay, will you use the door lock solenoid if your drives have them, what value will you select for the head load time, will you set up your drives so that the head loads with drive select or head loads with motors on, if there is no head load line on your drives, will you implement the automatic deselect all feature, and will you poll the deselect signal on the FDC-1 interface, etc, etc?

Of course the designers of this card have studied other published designs, and have found them mostly to be lacking in one respect or another. In summary the typical user is likely to be told "Well your drives are a bit non-standard and we didn't allow for them in our design", or worse: "Ours is working fine, if yours doesn't there must be something wrong with your drives". This is not what the typical Interak user will expect to hear. We are not infallible, and cannot claim to support everything weird and wonderful that has ever been invented, but we hope you can see that the most careful thought has been put into every aspect of the design to make it as excellent as we possibly can make it. (This design was working fine for us some years ago; during the following years all manner of embellishments have been added with experience, to try and make certain the design will work for you.

We now move on to construction, which will be less complicated than our earlier remarks will have lead you to believe. Despite its complexity the FDC-1 card is easy to construct because all of the difficult decisions can be postponed until after the soldering iron has been put away.

Good Luck!

By the way, before the card can be used there are some adjustments to be made. They are easy enough to make if you have (a) a screwdriver, and (b) an oscilloscope. The board may well work reasonably satisfactorily even if these adjustments are not carried out with meticulous accuracy, but we forbid you to fail to set it up perfectly - throw it away and go and buy a "home computer" it's all you deserve!

A setting up service is available for 25 pounds (+ VAT) if required, but this applies only to boards built exactly in accordance with these instructions. If you feel like leaving components out here and there because you don't need them yourself, or using your own choice of connector, you are at perfect liberty to do so, but if you get into trouble then you'll be on your own! We have enough trouble understanding these instructions and we wrote them so we have no chance of working out what you've done if you've decided to deviate from the straight and narrow.

3.1 CONSTRUCTIONAL NOTES

1. Read all documents very carefully before starting - just in case you later meet something you wish you'd known about before you started.

2. Read the notes given at the beginning of most of our manuals to see how to handle the Static sensitive chips safely. The two main such chips in this design are the FDC-1 chip itself and the 4066. If 74HC(T) series are supplied (these are only suitable for certain locations on this board so are not very likely to be) then these too must be handled with the full precautions. As it does no harm to follow anti-static handling precautions at all times with every type of chip, this is probably the best recommendation. As chip geometries get smaller and smaller more chips become static sensitive so one day all chips will be like this; we may as well get into training now.

   Identify all the components and using the Component Overlay and the Parts List, work out where they all going to fit before soldering anything.

3. The upper side of the board is the side which is visible when the card is viewed in the same way as is illustrated in the Component Overlay diagram, i.e. the diagram is drawn looking at the upper side. The other side is the under-side and the components are inserted from the upper side and soldered on the under-side, when the time comes. The two sides of the board are also known as the "A" side and the "B" side. These are identified by the letters "A" and "B" printed in the copper track near to the board's identification number. Insert the components through the holes on the ~~"A"~~ B side and solder them on the ~~"B"~~ A side.

   Note that this board has "plated-through" holes, so soldering is particularly easy (but errors are difficult to rectify so take care). Feed from the ~~"B"~~ A side the minimum amount of solder to make the joint all the way through the thickness of the circuit board, but do not let it flow out on to the ~~"A"~~ B side. To check, inspect on the ~~"A"~~ B side the joints made round the resistor leads. Underneath the ICs it is hard to inspect, and this is where the most damage can be done by too much solder.

4. Carry out any drilling or filing necessary to fit the card in the rack, and to bolt on the front panel. (This work should not be necessary, but if it were it would be a lot more difficult once the card had been assembled.) In order to get the longest life from the edge connector sockets in the rack it is vital to chamfer lightly all of the edges of the card around the gold-plated area and to apply a smear of suitable lubricant in use - but do not overdo either of these activities!

5. Check that there are no obvious defects on the board, e.g. damaged or short-circuited track etc. Look especially beneath

the IC socket positions since they will be hidden in the finished job.

6. Consult the Component Overlay, and the Parts List, to determine what goes where. Any convenient order may be followed, but a typical method is to start with the lowest height components and work up.

The Component Overlay and Parts List are located at the back of this manual for easy reference. Note that the Parts list is presented in two ways: firstly in order of reference number, R1, R2, R3, etc., and secondly in order of component value, 220R, 330R, 1k, 10k, etc. Probably the latter list is the more convenient for our present purposes, but the two separate lists have been prepared so that you can use the one you prefer.

Also great effort has been expended to number the components in sequence, ie in ascending order starting at 1. The numbers should be read as you would read a printed page, ie starting at the upper left hand corner and proceeding in horizontal rows. This should make it a lot easier than normal to work out what goes where without making mistakes.

The following steps can be used as a check-list:

(a) Fit resistors R1-25, (Note! Fit the correct values - the colour code is given in the Parts List.) They may be fitted either way round, but the maestro of the soldering iron will have all the resistors with the gold bands the same way round for neatness.

The correct way to bend the leads of the components is to hold them tightly with very fine pliers near the body, and to bend the free end. If you do it without pliers you run the risk of fracturing the joint between the wire and the body of the resistor. Annoyingly if this causes trouble it does not necessarily do so immediately, because the broken surfaces are clean and still making good contact; instead it can be a long time later that you get trouble, when perhaps the surfaces have oxidised or moved apart. Best is to spend the time now to do the job properly. (Of course a purpose made tool is best of all if one is available.)

Where a "-" is shown in the Parts List, this means that no resistor is to be fitted in the named position. Leave the holes unsoldered in case a resistor is to be fitted later.

(b) Fit the diode CR1. (Note! Fit it the right way round - see the Layout Diagram and the sketch on the Parts List. A particular trap, which has caught many a professional is those diodes which have a colour code for their marking. In this case it is the end which has the widest colour band which is the cathode, ie not the darkest nor necessarily the band nearest one end, but the widest band.)

Also note the remarks in the second paragraph of section (a) above. If anything there is more danger of damage to the diodes because the body is made from a glass-like material, which forms an hermetic seal.

(c) Fit IC sockets for DH12-3, U1-U24, and S12. Note that although there is space for DH1, DH4 and the upper left-hand "patch area" sockets are not normally fitted here. Be sure to use an acceptable type of socket if you are going to take advantage of the board supplier's fault finding service - see the Fault Finding Section of this Manual for extensive further remarks on this subject. Make the identifying mark on the socket correspond to the Pin 1 end of the DIL switch or IC. Do not plug any components into their sockets yet.

(d) Fit Y1, the Crystal. This should lie "prone" on the circuit board. Its leads should be bent using the same technique as decribed for the resistors in section (a) above, because of the risk of breaking the hermetic seal at the body of the crystal. If a double sided adhesive foam pad has been supplied with the crystal, use this to keep it in position while soldering, and to cushion the crystal in use. Holes have been supplied at each side of the crystal body so that a wire strap can be soldered over the whole crystal can to keep it firmly in place. Underneath the crystal is a crosshatched earthed area for screening. This need not make contact with the crystal can, but it does not matter if it does.

(Note! The crystal is fragile; do not drop it. It is sensitive to heat; try and hold the leads with pliers between the body and the soldering iron to shunt the heat away. If you can't manage this easily, at least solder it quickly and cleanly. There are numerous holes for different oscillator configurations with the result that the crystal can be mounted in two places; use the left hand set of holes. Position the crystal so that it is not so high as to foul the card guides when the board is plugged in, but not so low that it is near the unused component holes which are dangerously close to the crystal body, particularly the one which is 0.1" due north of end 2 of the crystal.)

(e) Fit C1-31. (Note! C1-4, C25, C29, and C31 are polarised types which must be fitted the correct way round. The "+" lead of the capacitor will be marked "+", or can be identified by a process of elimination as being the lead which is not marked "-".) Consult the sketches in the right-hand column of the Parts List (at the back of this Manual) for further guidance. If you are not used to capacitor markings go through the whole list of capacitors, comparing the different types and quantities supplied, until you are sure you know which is which.

C17 and 18 deserve special mention. They must be 100nF

polyester. The vast majority of capacitors are described as "Dec" which stands for a general purpose decoupling capacitor of value between 47 and 100nF. Often C17 and C18 will be obviously different from the decoupling capacitors as they are of better quality, but equally often the decoupling capacitors supplied will be of the same quality. If the decoupling capacitors are the same as C17 and C18 of course it does not matter which is used for what, and if they are obviously different then it is easy to pickut C17 and C18. One source of confusion (which we will try to avoid of course when packing the kits) is when assorted 47nF and 100nF are supplied. Because they look the same you may not notice the slightly different markings, and you might accidentally install the capacitors intended for C17 and C18 in the "Dec" positions. Therefore our advice is to identify C17 and C18 before you begin.

Where the symbol "-" appears in the parts list it means that no capacitor is to be fitted in that location. Leave the holes unsoldered in case a component should need to be fitted later.

(f) Fit CV1, the variable capacitor (trimmer). Because there are many different patterns of trimmer there are numerous holes provided for this component; use the ones which seem most appropriate. With a 3 pin trimmer the bottom two leads are shorted together, so make sure your choice of holes provides for this by looking at the tracks on the board.

(Note! These trimmers are often of "open" construction and care should be taken not to inflict any physical damage on their fairly delicate component parts.)

(g) Fit the four 9-pin 0.1" socket strips which are used as sockets for SIL1-4.

One type of socket-strip which may be supplied is just like half a dual in line (DIL) integrated circuit socket, and should be fitted in the same way as such a socket.

The other kind of socket strip comprises a number of formed sockets on one-piece carriers. Do not break off the carriers yet! Solder the strips in position and when you are sure everything is correct, and only when, break off the carriers by bending them gently back and forth with long nosed pliers, being certain not to distort the socket parts in any way.

Do not be tempted to discard the sockets and solder the SIL resistors in directly. The SIL resistors are cheap enough not to merit sockets, but sockets are provided so that the resistors can be unplugged easily and changed for other values should the need arise.

(h) If an IDC ribbon cable connector for the disk interface is

to be fitted directly on the card in position J1 install it now.

Although a 34-way could be used, a 50-way type is recommended most strongly so that the FDC-1 card is truly universal (it is easy enough to organise things so that a 34-way ribbon cable can be plugged into a 50-way connector, but impossible the other way round!) If you insist on using a 34-way connector (not recommended) then be sure to put it in the upper group of holes, ie its pins 1-34 corresponding to pins 17-50 of the 50-way type. (Don't ask me to explain the logic of this - you will have to ask a disk drive manufacturer why pins 1-34 on a 34-way cable weren't arranged to correspond with pins 1-34 of the existing 50-way cable, I only know they weren't!)

Bolt the connector (if used) into position and check it is correct before soldering. If the connector is to be mounted on a front panel and connected via the (optional) set of 0.1" pitch pin assemblies then these pin assemblies can be fitted as part of task (i) next. If you are uncertain which type of connection method to use it is safe enough to solder a connector straight to the card; if a front panel type is required later direct cannections can still be wire wrapped to the connector soldered on the card.

(i) Fit the 0.1" pitch pin assemblies P1-P19 (these comprise 17 3-pin and 2 4-pin assemblies, as indicated on the component overlay diagram, immediately before the parts list at the end of this Manual.) Pass the short length of the pins thorough the card from the top and solder on the under-side, like all the other components. (For very low-profile work they can be mounted upside down, i.e. the long ends through the card, and the surplus cut off after soldering, but there is no point in doing this on this card.)

(j) Fit the 4 potentiometers RV1-4. These should be the upright square multiturn type. Although no great disaster results if they are each connected wrong way round (but note there are two values 10k and 50k which should not be confused), try to fit them with pins 1,2,3 in that order. Care has been taken in the board layout so that you turn clockwise to increase the setting, and you will undo this good work if you insert them the wrong way round. You will see that there are two parallel sets of holes for each one; this is to accommodate the two main types of potentiometers available, one has its leads in the centre, the other offset to one side. As the components nearby are now in position you can try alternative positions for RV1-4 to see which looks the best before soldering them.

7. Install the DIL switches S1 and S2, and SIL resistors SIL1-4. The DIL switch is to be fitted the same way round as the integrated circuits will be, ie with end 1 upwards. (Note! SIL1-4 must also be fitted right way round; pin 1 of the SIL Resistor

packs will be identified in some way, often with a hardly visible dot nearer the pin 1 end than the other.)

(The integrated circuits and DIL headers are not be fitted yet. If the sockets are at any risk of contamination cover them up with say masking tape.)

8. If you wish, use a suitable solvent to remove any flux deposits from the track side of the board. (Note! Some solvents also dissolve some types of plastic, beware particularly of J1, RV1-4 and S1-2.) Also note that over-zealous use of flux-removing solvents can actually cause trouble, by washing impurities into connectors and IC sockets. You can give some protection by covering them with masking tape, but in many cases it is better to ignore this step altogether. Nevertheless because of the long-term harmful effects of flux left on circuit boards a board assembled to our approval will have the flux removed.

9. If a metal front panel is to be fitted (which is recommended) and a front panel connector (which is at your option - whether or not you choose this depends on whether or not your disk drives will be inside or outside the computer case) cut out the slot for the ribbon cable connector plug J1, according to the drawing provided in the Diagrams Section of this Manual. (Note! Take care to avoid scratching the metal card front).

10. Fasten all of the front panel components (brackets, handle, and J1 if panel mounted) to the front panel.

11. If J1 is front panel mounted connect it to the appropriate places on the board, (ie to the same numbered connections as would naturally result if a pcb mounting connector had been fitted) using a wire wrapping tool and wire.

    Wire-wrapping is the recommended method of connecting the front panel connector to the pin assemblies on the FDC-1 card. Another method is to use special push on crimped connectors, or even, if you have no alternative, soldered connections directly to the pin assemblies.

12. There are various links to be made (and not made) on pin assemblies P1 to P19 but as they will undoubtedly be different for different users, precise guidance will be deferred until section 3.2 next (Setting up and Testing).

13. If desired the board may be lacquered on the under-side. A suitable printed circuit board lacquer should be used, and similar precautions should be taken as described in the earlier paragraph (no. 8), to prevent the connectors and IC sockets from becoming contaminated. It is probably safest to ignore this step if you are in any doubt, as a lot of damage can be done through lack of experience here. (Note! be sure not to lacquer the gold-plated edge connector on the card, and mask the pin assemblies as well.)

3.2 Jumper Link Settings and Options

The following notes describe how the FDC-1 Jumper Link Settings and Options can be decided upon. They only refer to the FDC-1 board itself, but it is of course equally important that any options on the disk drives themselves be set up appropriately. A future issue of these notes will attempt to give specific guidance on these "outside" matters, as we first need to gain the experience of seeing what difficulties are met in practice by users purchasing their drives on the surplus and second hand markets. Naturally if we are able to supply the drives ourselves we will have full information.

In addition to the designated "P" number pin assembly areas there are several others (DH1,2,3,4, S1,2) where arrangements have been made for options, address selection and the like. As the card may be used as the disk controller in finished ("ready made") systems produced by various manufacturers, who all have their own individual preferences, as wide a choice as possible has been provided to make these connections.

The cheapest way of all, but not recommended, (certainly your Interak supplier will not accept such boards for testing and setting up without an enormous surcharge!), is to wire in permanent wire links. Another, more acceptable, method is to fit more of the 0.1" pitch pin assemblies and make the connections with shorting jumper links ("J-Links"), but the recommended method is to fit nothing in positions DH1,4, DIL sockets and plug in 16-pin DIL headers for DH2,3 and DIL sockets and DIL switches (8 x SPST) for S1,2.

(However if you are not building from a kit and if it suits your manufacturing style you can use whichever of these techniques you prefer: most, if not all, of the connections are made in straight lines at each area which makes the use of DIL switches or J-Links feasible. J-Links which are provided but not needed for the particular configuration in use can conveniently be "parked" on adjacent 0.1" pitch pin assemblies, if you solder some more in.)

(Two of the connection areas allow for modifications and alterations which are not likely to be required in all normal uses of this card and the preferred connection has been hard-wired in the copper track, which must therefore be cut before alterations are made. No more guidance will be given on this as no known normal implementation of the disk controller will require them. These two areas are DH1, and DH4; no components should be inserted here.)

Many users however will not have any strong views on the subject and will prefer more specific guidance. The standard kit of parts includes the recommended hardware for this purpose and should be installed and used as follows.

DIL Header Plugs DH2, DH3

The only part of the setting up procedure not covered in the present issue of these notes is what connections to make on the DIL (dual in line) header plugs, DH2 and DH3. To decide what do here use sheet 2 of the circuit diagram (Manual Section 5). The pin numbers of the interface cable to the disk drive are given on the left-hand side of the drawing, and the signal names to the right. All you have to do is decide what links should be made on DH2 and DH3 to connect the signals on your specific disk drives to those of similar name and identical function on the FDC-1 board. A lot of thought has been put into the

design of these headers so that in the majority of cases simple straight line links are all that are required. For example for most 8" drives (which are the most "standard" of all disk diameters) 4 straight links are all that are required. These are on header DH3 and link the following pins: 1-16, 3-4, 5-12, 7-10.

In the two areas near the main input connector, it is recommended that 16-pin sockets be used and the connections made via wires soldered to a plug in header. The common arrangements for 5" and 8" drives have been studied, and it is hoped that their needs can all be met by fitting or omitting straight wire links on the header. If this is a vain hope then you should nevertheless still find some method of making connections you require on the headers even if now the wires have to be crossed.

DIL Switches

There are two positions on the card where DIL switches are to be fitted; on the diagrams these are labelled S1 and S2. DIL sockets for these are supplied, although strangely many designers do not use sockets for DIL switches (even though being a mechanical component they are more likely to fail than an IC, and every bit as hard to remove once soldered).

The type of DIL switch to be used is 8 x SPST. Taking S1 as an example, we can therefore refer to eight switches S1a to S1h; oriented so that S1a would connect pins 1 and 16 of the socket if the pins were counted in the same way as for a 16-pin I.C. Very often the DIL switches themselves are numbered 1-8, corresponding to a-h in our notation. We have chosen to use letters rather than numbers because of the potential confusion of referring to say S1-2; it might not be immediately clear whether reference was being made to switch 1 of switch pack 2, or, switch pack 1, switch number 2.

DIL Switches S1a-e

The switches S1a-S1e (the first five switches of switch pack S1) select the I/O Port address. This will have to suit whatever software is in use; the settings for Interak 1 are given below. S1a is the MSD (most significant digit) and corresponds to the chosen state of address bus line AB7; the other switches continue in sequence for a total of 5 address lines until S1e is reached, which corresponds to AB3. Because the FDC-1 card uses eight I/O ports i.e. eight 256ths of the total number, then only 5 bits are selected. (5 bits because eight out of 256 = one out of 32, and only five bits are needed to decode one of 32, since each bit can have one of two states, 0 and 1, and $2^5=32$.)

Note that as EX-OR gates are used to select the chosen address (see circuit diagram Sheet 3), the complement of the address should be set on the switches, ie for an address with a "1" on a given line, the corresponding switch should be set to "0", by turning that switch ON. For example for use in a standard Interak 1 floppy disk system the ports used are 80H-87H consecutively. In binary notation this is 1-0-0-0-0-X-X-X, where the eight combinations of "0"s and "1"s in "X-X-X" represent the eight ports available for the FDC-1 Card. The required settings for S1a to S1e are therefore ON-OFF-OFF-OFF-OFF.

DIL Switches S1f-h

These three switches are the last three of the DIL switch pack S1. S1f-h are connected to Bits 7, 6, 5, respectively of the read buffer for Port "DCONR" (Port number 85H in a standard Interak floppy disk system).

By reading and acting on the state of these switches, the disk operating system can behave differently in minor ways, according to the wishes of the user. Since this depends so much on what an individual systems software author will prefer, and similarly the user's preference, the options here are likely to vary according to implementation. Details of these if needed should be included in the notes accompanying the disk operating system used.

If firm ideas emerge on the functions of these switches (and S2 described next) they will be published in "IUG" (Interaktion User Group) Newsletter.

DIL Switch Pack S2

This comprises 8 x SPST switches, S2a-g. When they are absent, or OFF, the associated logic levels rise to "1"s; "0"s are produced for any switches which are ON. The state of the switches can be examined by the software in use via the read port "DOPTS", which is at address 86H in an Interak Disk system.

Note that the present disk operating system software does not use S2, so it is immaterial how this switch is set. However, the switches have been provided for software purposes and may legitimately so be used in future, so you should consult the documentation supplied with the software for the definitive answer on this topic.

0.1" Pitch Pin Assemblies

There are several places on this card where 0.1" pitch pin assemblies, of length 3 or 4 pins, are to be fitted, either as test points for observing and measuring certain signals or as locations where options may be installed to suit particular types of disk drive or particular needs of the user.

The majority of these sites are used for setting the various options; the appropriate links are made by push fit shorting pieces or jumper links we call "JLinks". On each such assembly there is a "parking" position where a JLink not in use can be stored or "parked".

The remaining sites are used as test points and here it is vital that no shorting "JLink" be fitted. The pin assembly locations where no JLinks are to be fitted are numbered P5, P9, P15.

Also identified (towards the bottom left of the component overlay diagram, showing the card viewed on side "B" in landscape position) is one single hole "P20"; this is used on rare occasions as a termination point for a particular signal. In all normal use nothing should be fitted to "P20".

All of the other pin assemblies are numbered on the component overlay diagram,

starting at the top left hand corner of the board and continuing to the bottom right. The same numbers are used on the circuit diagrams.

P1, P2 (Circuit diagram Sheet 5)

As described later (see description of P4, P5, P12) an optional "Motors On" retriggerable monostable is provided on this card to keep the motors running for a little while after they have last been used, to save wasting time running them up to speed again if they are used soon after.

P1 and P2 set the period of the "Motors On" monostable:

P1 links	P2 links	Nominal Period	Typical Period
2-3	2-3	5 sec	4 sec
2-3	1-2	10 sec	8 sec
1-2	2-3	10 sec	8 sec
1-2	1-2	15 sec	12 sec

By altering the values of C1, C2, and C3, these times can be changed. The capacitor voltage has to be at least 5 Volts, but we prefer 10 Volts or more in practice, to allow a safety margin. The only limit to the maximum value of the capacitors you may substitute is that of their physical size. (Note that a single physically large capacitor can be accommodated in place of C1 and C2 by connecting it between the positive terminal pad for C1 and the negative terminal pad for C2, and linking P1 pins 1-2.)

Parking Position: Unused JLinks on P1 and P2 will have no effect if they are "parked" connecting linking 2-3 of each pin assembly, but see the note below.

Note: P1 pin 3 links U1 pins 6 and 14 to the 0V earth track. This is the appropriate connection for the negative poles of the capacitors when the specified 74LS123 monostable is used.

Normally leave P1 pin 3 linked to 0V, and use the specified component for U1.

Option: Sever the 0V connection to P1 pin 3. This disconnects the earth connection and allows you to substitute a monostable type 74123 to be used instead of the one specified, since the earth connection to the capacitors is not then required.

P3 (Circuit Diagram Sheet 2)

The first function to be discussed is that associated with pins 2 and 3 of this assembly.

Normally pins 2 and 3 are left open - this allows an artificial "Ready" signal to be produced by the half of the ic U1 shown on sheet 2 of the diagram. (The artificial "Ready" signal is produced by the monostable whenever a correctly timed stream of Index pulses are received from the drive in use. 8" drives usually generate the ready signal themselves so this circuit is of most use for 5" drives.)

Option: This is generally employed in 5" systems (ie those which are those most likely to be making use of the artificial Ready circuit) and allows a permanent

"Ready" signal to be produced (for example when developing system software). Link pins 2 and 3 to allow a permanent "Ready" signal to be produced irrespective of the state of the index pulses to the monostable. (The link between pins 2 and 3 short circuits the output of the U20 inverter to earth; this is perfectly in order because the inverter in question is an open collector type designed for such treatment and thus no harm will result.)

Parking Position: Pins 1 and 2 are permanently connected in track and so a JLink may be "parked" here when not in use. This corresponds to the "normal" state of affairs described in the paragraph before the one immediately above.

Note that the artificial "Ready" signal is of a very simple design (we do after all want to keep things simple [!]), and it is merely of assistance to let the operating software determine whether or not a diskette is mounted in the chosen drive, and that it is turning. When the software selects another drive the index pulse triggering the monostable comes from the new drive; as this is not necessarily in synchronism with the original drive the output of the artificial "Ready" monostable cannot be relied upon until at least one revolution of the newly selected diskette has been allowed to take place. The circuit does not have sufficient precision to determine whether or not the diskette is turning at the correct speed; it merely indicates the presence of a rotating diskette.

P4 (Circuit Diagram Sheet 5)

Normally: Link 2-3 to allow the output pin 5 of the "Motors On" retriggerable monostable U1 to control the "Motors On" output to the disk drive. (The action is that a port output (write) to the latch (U16, type 74LS273) on page 5 of the circuit diagram will trigger the monostable, which in turn will keep the disk drive motors on for a few seconds so that no time need be wasted restarting them should further disk activity be forthcoming.)

Option: Fit no link, or fit it to link 1-2. The pull up resistor R6 then will hold U7 pin 1 permanently high and U7 output pin 2 will be permanently low keeping all motors on at all times.

Parking Position: As 1-2 are linked by copper track on the board this makes a suitable position for parking a JLink. The effect then will be to select the "Option" decribed above.

(Note: if pins 2-3 are linked then once the motors on momostable has timed out the latched state of DAL6, (ie at U16 pin 2), is able to keep the motors on under direct software control; however the usual arrangement is to set the latched state of DAL6 to logic "0" so that the state of the motors depends entirely on U1 pin 5 and the settings of the P4 pin assembly.)

The purpose of the resistor R6 connected to pins 1 and 2 of this pin assembly is to ensure that even if no JLink is fitted U7 pin 1 will never be left "floating", ie it will always be connected to a known logic level.

P5 (Circuit Diagram Sheet 4)

This is a 4-pin assembly which is used only for test points and so should never be linked in any way.

Normally: Test points - must not be linked.

(Part of Test Procedure repeated below for the reader's convenience):

Press Reset or Output to Port 85 data 00, i.e. 5" D/D

Pin 1	f = 4.00 MHz; T = 250 ns
Pin 2	f = 2.00 MHz; T = 500 ns
Pin 3	f = 1.00 MHz; T = 1000 ns, i.e. 1 us
Pin 4	Logic "1"

Output to Port 85 data 04, i.e. 5" S/D

As above, namely:

Pin 1	f = 4.00 MHz; T = 250 ns
Pin 2	f = 2.00 MHz; T = 500 ns
Pin 3	f = 1.00 MHz; T = 1000 ns, i.e. 1 us
Pin 4	Logic "1"

Output to Port 85 data 08, i.e. 8" D/D

Pin 1	f = 4.00 MHz; T = 250 ns
Pin 2	Logic "1"
Pin 3	f = 2.00 MHz; T = 500 ns
Pin 4	Logic "0"

Output to Port 85 data 0C, i.e. 8" S/D

As above, namely:

Pin 1	f = 4.00 MHz; T = 250 ns
Pin 2	Logic "1"
Pin 3	f = 2.00 MHz; T = 500 ns
Pin 4	Logic "0"

Parking Position: Test Points Only - no parking for JLinks.

P6 (Circuit Diagram Sheet 5)

This allows the option of "auto deselect" of all drives when the motors-on monostable times out. Whether or not this feature is used depends entirely on the combination of operating software in use and the user's own personal wishes.

Link 1-2: this routes the "not-Q" output of the motors on monostable U1 to the U3 enable pin 14. Whenever the monostable is triggered, ie holding the motors on, one or other of the drive selects (taken from U3 pins 9, 10, 11, 12) are active according to the state of the signals "BIT 0" and "BIT 1", ie the inputs to U3 pins 13 and 3. As soon as the monostable times out U3 pin 14 goes to a logic 1 automatically deselecting all drives.

The thinking behind this is to prevent a drive remaining selected while its motor has come to rest: if the drive had the option "head loads with select" and this were chosen by the user then it would result in the head remaining

loaded on a stationary diskette. (There is no direct evidence that this is a bad thing, but some experience in similar circumstance with magnetic tape shows that physical creasing of the magnetic medium can result, or demagnetisation and loss of data owing to residual magnetism in the recording head. Obviously not a happening with which to take chances, although it is unavoidable with those drives which do not have a mechanism for unloading the head when a diskette is mounted. Unless "tram lines" are to be engraved into the diskette surface, and the head worn prematurely, it will have to be accepted that the motor be turned off with a diskette still mounted, even though the head is still loaded.)

Link 2-3: this disables the "auto deselect" feature and leaves U3 pin 14 permanently enabled. Whether or not the drives remain selected now depends on the state of the latched output "Deselect All (H)" U16 pin 16. (Logic 1 - high - to deselect all drives.) This option is used both for testing, and for certain specific software which does not require the auto deselect feature.

Parking Position: None required; a JLink is always fitted, linking either 1-2 or 2-3.

Note: Whatever the position of the Link on pin assembly P6, the "Deselect All (H)" signal is always capable of deselecting all drives if it is set to a logic 1 (high). It is not as easy for typical disk operating system software to perform the same function via the "Deselect All (H)" line as does pin assembly P6, because this results in a lot of undesireable "head banging". This is because the relevant part of the software is not able to predict whether or not the record it is reading or writing is the last of a sequence so it would always have to play safe and leave the drives deslected, thus unloading the heads. If, as would normally be the case, the record being written were not the last of a series then the appropriate drive would be immediately selected again, banging the head down excessively. Most systems software authors choose the "Deselect All (H)" line to be left at logic 0 (low), being set high only in the most distressing circumstances, for example if after numerous retries the system software is not able to read a diskette which it should have been able to read.

P7 (Circuit Diagram Sheet 5)

This pin assembly controls the state of the "Lock Doors (L)" output from U15 pin 6, by selecting the signal for U15 input pin 5.

Normally: Link pins 1 and 2, to allow the latched state of the DAL6 bit (U16 pin 19) to control the "Lock Doors (L)" output to the disk drive. Whether or not the doors are locked will then depend on the controlling software. (Note that many drives lock the doors automatically whenever the head is loaded; this is a separate function to the explicit "Lock Doors" signal. Equally many drives do not have the necessary internal arrangements to allow them to obey this signal, and are incapable of locking the doors on demand.)

Option: Link pins 2-3 to ensure that the "Lock Doors (L) signal is never activated, regardless of the latched state of the DAL6 bit (U16 pin 19). This disables the software control completely and makes it impossible for the software to lock the doors. (This option could be used for example during a debugging phase of software development to overrule recalcitrant software.) This option is often used to defeat software which has been written to lock the

doors at every available opportunity. Excessive door locking is quite irritating to the knowledgeable user since he would never open the door on a drive in use anyway, but he certainly does not want to suffer the substantial mechanical noise of a solenoid operated door lock. The "normal" recommendation given above has been chosen so that the capability exists to lock the doors by writing appropriately to the DAL6 bit to be latched in U16 and to allow the software to lock the doors in some exceptional circumstance (eg when data is particularly at risk, or for safety or security purposes when children or unauthorised users are operating the machine).

Parking Position: None required; if used, the JLink is always connecting either 1-2 or 2-3.

P8 (Circuit Diagram Sheet 5)

Normally: Link 1-2, allowing the Reset signal (the same as is used for the Floppy Disk Controller chip) to reset the 74LS273 latch to a known state of all 0's, i.e. default to 5" Double Density.

Option: With Link 1-2 removed, a momentary connection from pin 2 to pin 3 will then reset the latch to all 0's (should this be required for some esoteric test procedure). Alternatively, permanently leaving the pins open (ie allowing the pull up resistor R10 to take control) will allow the latch to retain data regardless of the state of the system reset line, again only of use for some odd test procedure. (Finally, if pins 2 and 3 are permanently short circuited the recommended 74LS273 can be replaced by a 74LS374 should the correct chip be in short supply. However if you do make this substitution note that the 74LS374 has no reset pin and an appropriate output to port 85H instruction must be issued very early on in the operating software if known initial behaviour is to result.)

Parking Position: None required. In the majority of normal and optional uses a JLink is always fitted, either to 1-2 or to 2-3.

P9 (Circuit Diagram Sheet 6)

These are test points only and so should never be linked in any way.

Normally: Test points - must not be linked.

Once the Controller Chip has been set into its Test Mode, the pins bear the following signals. (A brief summary of the setting up procedure, given in detail elsewhere in this manual, is also presented):

Pin 1 Precompensation pulse width for double density (commonly set to 150-200 ns). 5" setting adjusted by RV1 and 8" by RV2.

Pin 2 VCO centre frequency -adjusted by CV1.

Pin 3 Read pulse width, (depends on selected diskette type (5" or 8" S/D or D/D)

5" S/D adjust RV3 for 1 us (1000 ns)
5" D/D adjust RV3 for 500 ns
8" S/D adjust RV4 for 500 ns
8" D/D adjust RV4 for 250 ns

Parking Position: Test Points Only - no parking for JLinks.

P10 (Circuit Diagram Sheet 7)

Although the FDC-1 card and all related software are designed specifically for the 2797 type of floppy disk controller chip, some consideration has been given to the possibility of substituting a related type, the 2793. (In this design the 2793 is inferior as the design then cannot cope with true double sided diskette operation, however this may not worry those users who have only single sided drives.)

The two FDC chips (U11) differ in the function of pin 25. On the 2797 this is an output called "Side Select", on the 2793 it is an input which has the function of allowing an internal divide-by-two of the clock input pin 24. This function is redundant on this board as it is carried out externally, by U10, the 74LS107. Pin 25 of the 2793 has its own internal pull-up resistor and defaults to the 2797 mode when this input is left open circuit.

Normally: 2797 chip fitted, 1-2 linked to conduct the "Side Select" output to the disk drive interface via U20 pins 3 and 4.

Option: When a 2793 chip is substituted for the recommended type, its pin 25 is taken high under the action of its internal pull up resistor. The state of the "Side 1 Select (L)" signal is now no longer under the control of the FDC chip U11. This would generally thought to be of no concern if a 2793 chip were in use as the 2793 is not designed to cope directly with double sided drives, but in the event of a double sided drive being connected to what is now a single sided controller it may be of importance to the user to choose which of the two available sides is to be taken as the single working side. Usually it will be side 0 which is chosen for this purpose and P10 should normally be linked (when a 2793 is in use) so that pins 2-3 are connected. In the rare circumstance that side 1 of the diskette is to be used for single sided working then P10 pins 1-2 should be linked. U20 pin 3 will then be taken high (under the action of the internal pull up resistor at U11 pin 25) which will cause the output of U20 pin 4 to be low so activating the "Side 1 Select (L) interface signal.

Parking Position: None required: a JLink is always fitted linking either 1-2 or 2-3.

P11 (Circuit Diagram Sheet 7)

This is an input to the FDC chip which sets it into a special mode called "Test", which is an essential part of the initial setting up procedure. This mode allows certain internal signals to be output to pins which normally have different functions. (A summary of the outputs on test has already been given, under the description of P9.) If pins 1-2 are linked, (or if no link is fitted, allowing pin 2 to be pulled high under the action of an internal pull-

up source in the FDC chip U11), the chip is in its normal operational mode; pins 2 and 3 should be connected to enter the test mode and should remain connected while all the tests and adjustments are carried out.

Normally: link 1-2, which can also be thought of as a "parking" position. If you have a JLink of a different colour from the others use it here to make it easier to find this particular link during testing.

Test: to enter the test mode operate the system reset (usually a switch on the CPU card) and link 2-3. To leave the test mode remove the JLink , parking it on 1-2 if preferred. See note below.

Note: While pins 2 and 3 are linked do <u>not</u> allow the controller chip to be reset - this enters yet another mode, not used in this design, which switches off the internal Voltage Controlled Oscillator, allowing an external one to be substituted, eg if this FDC chip was being "retro fitted" to a card designed with the earlier FDC chips which did not have internal VCOs. (If this mode is entered accidentally, normal operation can be restored by removing the JLink 2-3, replacing it on 1-2 if desired, and resetting the FDC chip, eg by operating the system reset switch.)

<u>P12</u> (Circuit Diagram Sheet 4)

This is associated with the "Motors On" monostable function, already mentioned under the descriptions of P1, P2, P4, P6.

The use of motor control saves power and a certain amount of wear on the disk drive motors, but is a little more harsh on the diskettes themselves and other parts of the mechanism, because the diskettes and other parts are repeatedly subjected to violent speed variations when the motors turn on and off. As with motor cars, "stop start" operation can in fact be more wearing than continuous operation.

Most 8" drives, and an encouragingly large proportion of modern smaller diameter drives, are rated for continuous motor operation (with the head unloaded of course), and this obviously gives the fastest possible response to calls for data from the disk drives. However some users have a prejudice against continuous operation (perhaps owing to experience of motor reliability problems with early cheaply constructed drives, particularly 5"), and such operaton is most undesirable with those types of drives which do not have a mechanism to unload the head on a mounted diskette when the drive is not in use.

If continuous operation is to be avoided, the explicit "Motors On (L)" signal can be used in the disk drive interface, in conjuction with the "Motors On" monostable (U1 on Circuit Diagram Sheet 5). However, in such a circumstance it is very desirable that there be a way for the disk operating software to determine whether or not the motors are still running under the control of the Motors On monostable. (If the software were unable to do this it would have to play safe and assume that a second or so's delay be allowed at every disk access for the motors to be started up again. As this could happen many many times during the accessing of just a single file on the diskette, this would cause an unwarranted considerable slow down in performance.) Linking P12 pins 1-2 allows the state of the U1 monostable "not-Q" output pin 12 (Circuit

Diagram Sheet 5) to be tested, to see whether the motors are on or not. And equally importantly, if the "Auto Deselect" function, (discussed previously under the description of P4), is used then the same test will allow the software to avoid immediate access to a drive which has been deslected and whose motor may have come to rest.

If continuously operating drives are in use P12 pins 2-3 are linked, which can be taken as equivalent to a permanently retriggered Motors On monostable.

Thus:

Link 1-2: This is used if the motors on monostable and/or auto deselect functions are in use (see the descriptions of pin assemblies P1, P2, P4, P6 for more details), and lets the software determine the state of the monostable by reading bit 4 of the appropriate port (often Port 85H) via the internal bus DAL4.

Link 2-3: This is used if continously running motors are used, or if the tests described are carried out some other way (see "Note" below), and when the state of the Motors On monostable is thus immaterial.

Link neither: This is not used for normal operation but it is very useful in the phase of software testing in order to see what behaviour and how much delay results if the Motors On monostable signal is artificially distorted to the extent of appearing permanently timed out.

Parking Position: None needed. In all normal operation a JLink is fitted either to pins 1-2 or to 2-3.

Note: There are other ways for the operating software to determine whether or not a disk drive is ready to use, or if its motor has slowed or stopped. The trivially easy way if 8" drives are used is to test the "Ready" signal produced by the drive especially for this purpose, but as this signal is generally not available for the smaller diameter drives another, much cruder, method can be used. That is to try and read an ID field from the diskette (this is in any event the natural first operation before reading or writing data is attempted). If the chip indicates an error, it can be argued that possibly the drive is not ready, which is pretty well confirmed if subsequent retries get the ID field without error. Also available to the software designer is the "Artificial Ready" signal which is produced by the part of U1 monostable shown on Sheet 2 of the Circuit Diagram. This is not sophisticated enough to give an accurate indication of whether or not the speed of rotation is correct (accuracy which is expected of the "Ready" signal from an 8" drive), but it certainly can be used (with care, especially when switching from one drive to another) to indicate whether or not a diskette is mounted in the drive and is rotating.

Further Note: If motor control is provided on 8" drives, it appears generally to be the case that they cannot accept the single "Motors On (L)" line provided in the 5" interface. Often instead 4 individual lines are provided, sometimes with the inconvenient polarity that a logic 0 on the interface cable means "Individual Motor Off" rather than "Motor On". As the FDC-1 card is already embarrassingly over-endowed with options, it was decided that it was not practical to add the extra complexity of quadrupling the existing motor control arrangements (to say nothing of the author's difficulty in describing this further complexity). However the wise (for once) manufacturers of the disk

drives in question allow an option of "Motor On when Drive Selected", or "Motor On when Head Loaded", so it is an easy matter to get the appropriate motors on.

A convenient addition provided in the design of the particular 8" disk drives which have been studied is that they have their own optional internal Motor On monostable, which keeps the drives running for several seconds after the last time they were used. If the "Ready" signal from such a drive is examined, it is an easy matter for the operating software to determine whether the motor is still running or not, and so avoid a possible start up delay, but the use of the 1-2 option on this pin assembly can also be used: If the settings of P1 and P2 are chosen appropriately, so that the time period of the Motors On monostable on the card is just slightly less than that of the similar monostables in the disk drives themselves, it is just as effective for the operating software to test this on board monostable to infer whether or not the motors are being held on by the disk drive's own monostables.

P13, P14 (Circuit Diagram Sheet 6)

These set the time constant for the monostable which sets the head load time. The correct setting depends on the disk drive in use and will be specified by the disk drive manufacturer. If the exact time required is not shown below then use the next longest time. The times shown below are calculated nominal values, and should be confirmed by measurements on the board when it is working if the most accurate setting-up procedure is desired.

The head load monostable merely allows time for the head to settle on the diskette before reading is attempted. There is no great penalty to be paid if it is slightly wrong: if it is too short the read error which results will cause the disk controller to re-try and if it is too long a few milliseconds will be wasted after the head has settled when it is not being used. Obviously just right is best, but we recommend that you err on the side of providing a longer setting if you have to err at all.

P13	P14	Equivalent Timing Resistor	Head Load Time Calculated	Typical
1-2	1-2	8.2k	37 ms	30 ms
1-2	2-3, (or none)	11k	50 ms	40 ms
2-3, (or none)	1-2	13k	60 ms	50 ms
2-3, (or none)	2-3, (or none	22k	100 ms	80 ms

Parking position: Linking 2-3 has the same effect as fitting no link so this can be considered as the parking position in each case.

P15 (Circuit Diagram Sheet 4)

These are outputs and No links should be made. Pin 1 is an open collector output which goes low when the FDC output signal DRQ is high, and Pin 3 goes low when INTRQ from the FDC chip goes high. Pin 2 has no connection. These outputs are provided for experimental use, (for example to the direct connection to the interrupt request line(s) or direct memory access line(s) in systems which service the floppy disk card using those methods). Fortunately the Z80A CPU is one of the few processors which is fast enough to be able to

use a polling technique and so not need this additional complexity, even at the very high data transfer rate required by 8" double density, which is twice as fast as the 5" double density rate which is the maximum many current computers can tolerate.

If pull up resistors (say 1k) are added to pins 1 and 2 they can also be used as test points for the signals mentioned; note that as U20 is an open collector device no signals can be observed without the resistors.

Normally: make no connections here and fit no JLinks.

Parking: No Parking allowed.

P16: (Circuit Diagram Sheet 7)

This is a "Local Reset" function. Momentarily linking pins 2-3 will allow the circuits on this card to be reset independently of the system (however the 74LS273 latch on circuit diagram sheet 5 will only be reset if P8 pins 1-2 are connected). This feature has little practical value, except perhaps for some test purpose during some arduous fault finding session with inadequate software.

Normally: Link 1-2 (or make no links).

Parking Position: 1-2.

P17 (Circuit Diagram Sheet 6)

This, together with P18 and P19, select the desired write precompensation arrangements.

If no links are made on P17 write precompensation is applied permanently - this is an option which is never required so a JLink is invariably fitted as follows:

Link 1-2: If pins 1-2 are linked precompensation takes place according to the description given under the headings "P18" and "P19" later.

Link 2-3: If pins 2-3 are linked no precompensation is applied in any circumstances, for example link 2-3 if only single density encoding is used, or if you are using disk drives which genuinely do not require precompensation, but note that precompensation usually does no harm even so, and can do some good. (Another use is for test purposes, when it is deliberately desired to make a bad diskette in order to try out say the error recovery routines in the operating software: be sure to return the link to its correct position after such experiments are complete!)

Normally: link pins 1-2 and see "P18 and "P19" next.

Options: as discussed above.

Parking position: none required; in normal use a JLink is always fitted in one position or another.

P18: (Circuit Diagram Sheet 6)

These two assemblies are used in conjunction with P17 (q.v.) and select various write enable precompensation arrangements as described below. (The amount of precompensation is selected by the user by adjusting the RV1 and RV2 potentiometers, for 5" and 8" respectively, during the setting up procedure. The disk drive manufacturer should provide guidance to determine the amount needed, and knowledgeable users can set up an experiment to find it out, but in the absence of other data 150 ns and 200 ns are reasonable guesses for 5" and 8" drives respectively.)

If precompensation is used, it is generally applied at tracks numbers greater than that at the half way point, so that it is the innner tracks which get the precompensation. The chosen FDC chip has a signal called TG43 (Track greater than 43) which is in fact the optimum place to begin compensation on 8" diskettes which have 77 tracks in all. This signal can control the U11 ENP (Enable Precompensation) input pin 1 directly if 8" drives alone are used. This method would also be near enough for 5" 80 track drives, but of course would not be suitable for 35 or 40 track drives. The latched data line DAL4 (see U16 pin 5, Circuit Diagram Sheet 5) produces a signal which can perform the required function (given suitable controlling software) for any chosen number of tracks.

There is consequentially quite a variety of options, and these are detailed below.

Link P18 pins 2-3: With this option the precompensation is exclusively under the control of the operating software via the ENPSEL (H) line, and in this case the software should be written to suit the drives and formats in use. With P18 pins 2-3 linked the state of the links on P19 and the FDC chip signal TG43 is immaterial.

Link P18 pins 1-2: This achieves automatic control via the TG43 output from the FDC chip U11; precise details depend on the state of the links on P19 (and the current disk drive diameter in use), and the FDC chip output signal TG43; these are discussed further under the heading "P19" next. Note that in this position the software control line "ENPSEL (H)" is still able to add precompensation at track numbers 42 or less. "ENPSEL (H)" should be held at logic 0 if this is not desired.

Parking Position: Not required: A JLink is always fitted in one of the two positions 1-2 or 2-3.

P19: (Circuit Diagram Sheet 6)

This is a 4-pin assembly.

(Note that the links on this pin assembly only have significance if P18 pins 1-2 are linked and the "ENPSEL (H)" line is at logic 0. Should "ENPSEL (H)" be logic 1 at any stage, precompensation is applied regardless of the state of links on pin assemblies P18 and P19.)

Link 1-2 (With also a JLink connecting P18 pins 1-2): This provides automatic precompensation at tracks greater than 43 for 8" drives only; no

precompensation is applied automatically for 5" drives (thus in this case 5" precompensation if required has to be applied by asserting the "ENPSEL (H)" line under the action of the controlling software.)

Link 2-3 (With also a JLink connecting P18 pins 1-2): This provides automatic precompensation at tracks greater than 43 for 5" drives only; no precompensation is applied automatically for 8" drives. (If 8" precompensation is required this has to be applied now by the controlling software which has to assert the "ENPSEL (H)" line whenever precompensation is to be applied.)

Normally: link 3-4 (And P18 pins 1-2) This provides automatic precompensation at tracks greater than 43 for both 5" and 8" drives. This setting would be used for example for a mixture of 5" 80-track drives and 8" 77-track drives. It is also the appropriate setting if 5" 35 or 40-track drives are used as well, in which case precompensation for these (if required) has to be applied by asserting the "ENPSEL (H)" line under the controlling software.)

Summary of links on P18 and P19: The Links below result in write precompensation at tracks greater than 43 (but note that in every case the signal ENP SEL from the operating software overrules, providing P17 pins 1-2 are linked).

	P18	P19
Automatic precompensation for 8" tracks greater than 43	1-2	1-2
Automatic precompensation for 5" tracks greater than 43	1-2	2-3
Automatic precompensation for both 8" and 5" ditto	1-2	3-4
Automatic precompensation for neither 8" nor 5"	2-3	(any)

Parking Position: Not required: either the position of the link on P19 will be immaterial, or one of the 3 possible positions (1-2, 2-3, 3-4) will always be required.

P20 (Circuit Diagram Sheet 2)

This is simply an identification for an unused solder pad, which is connected to pin 12 of the interface connector for the ribbon cable to the disk drives. (P20 is located 0.1" due north of end 1 of R19). It has been singled out for this attention because differing drive manufacturers are particularly vague as to whether this interface line is an output line or an input line, and what its function is. Discrete terminating resistors R17 and R19 have been provided so that they can be removed (by cutting) if P20 has to be used as an output, ie does not require input termination.

Normally: Ignore P20, and solder nothing to the pad.

Please advise of any errors found, or anything which is not clear - this is only a draft for the relevant section of the proposed manual.

D.M.P

3.3 Setting Up Procedures

Note on System Requirements

The minimum length of the reset pulse for the specified FDC chip is 50 us (microseconds). The typical value delivered on the Kemitron MZB-3 (CPU) card is 8 us so to stay within the FDC chip specification the MZB-3 card should be modified appropriately, eg by increasing its resistor R10 from 10k to say 100k. (Present experience with the first batch of FDC chips is that an incorrectly sized reset pulse does not seem to matter, (perhaps because the FDC-1 card incorporates a power-on reset circuit which gives a proper length reset) but it is sensible to comply with the published specifications throughout to be sure of good results, and so this change is strongly recommended. Note that the change to the MZB-3 card does not cause any system difficulties, in particular the correct refresh of dynamic RAMs is not prejudiced by the lengthened reset pulse - the restrictions on dynamic RAM refresh is measured in milliseconds not microseconds.)

The highest rate of transfer of data occurs for 8" double density disks rotating at normal (360 rpm) speed, for 5.25" double density "8-inch compatible" disks (360 rpm), and for 3.5" double density rotating at double (600 rpm) speed. All other known systems transfer data at half or a quarter of the fastest rates. Many computers today (including the 16- and 32-bitters!) cannot cope with the highest data transfer rate. With suitable software in this design the Z80A-CPU operating at 4 MHz is one of the few which can, but only provided no "wait" states have been added in hardware. Wait states in a typical Interak System are introduced on the LKP-1 Card, and are set by small links. Remove them if you desire to operate at the highest rates. Of course it is not necessary to remove wait states in those areas of the memory map where the disk software is not ever to be used, for example in some special system which has non-disk software in EPROM, high up in memory, out of the reach of CP/M.

Setting Up and Testing

The setting up procedures and tests which can be carried out on this card are loosely classified as being either compulsory or optional. The compulsory ones are so named because (in general), the card will not work properly unless they are carried out. The optional tests have been devised to confirm that the major sub sections of the circuit on the card are sound. If the card is in perfect condition (ie there are no defects either in materials or workmanship) then all of the optional tests will be passed, and thus will prove to have been unecessary.

As some of the optional tests involve such procedures as removing integrated circuits and jumpering with wire from one signal to another, we think that on balance there is more harm than good to result when carrying them out and therefore it is our recommendation to carry out only the "compulsory" tests, and to omit the "optional" ones, unless circumstances (eg some difficulty in setting up or in actual operation) dictate otherwise.

To satisfy this recommendation the tests and procedures below are given in the order "compulsory" first and "optional" second.

A final few paragraphs before leaving this topic: All of our designs (software and hardware) to do with floppy disks are devoted to achieving the utmost reliability. If you commit your programs and data to disk, you have the right to expect that everything in the designer's power has been done to ensure that you can get this information back when you want it. Such techniques as "retries" are applied in the software so that should an occasional error be detected (such detection thanks to the constant vigilance of the FDC chip) many attempts at recovering the data will be made before the system gives up.

The purpose of this software mechanism is to cope with circumstances which are unavoidable, eg temporary specks of dust on the diskette, or misregistration of the disk head, all things which could correct themselves on the next revolution of the diskette. You will be able to see that the provision of such error recovery mechanisms will give protection not only against the unavoidable defects in the operation of a floppy disk system but also against defects which are avoidable. In other words there can be deficiencies on the board which are masked by the error recovery mechanisms: for example defective "enable precompensation" circuitry or incorrect "head load monostable" timing components. (This incidentally could be the explanation why the manifest defects in some commercial disk based systems, eg intolerance to certain makes of disk drive and diskettes, were allowed to get out into production - the errors in design simply were not noticed until it was too late.)

The difficulty is that there is no clear cut distinction between an acceptable system and one which is not; it is all a question of statistics. In a perfectly set up system with brand new disk drives and diskettes the odds may be millions to one against receiving irrecoverably bad data, but if the various safety margins are eroded, eg by defects on the FDC card, or just mechanical wear and tear, the odds shorten, and failures will become more likely. The purpose of the "optional" tests is to expose faults which otherwise may not be obvious, so you may prefer to execute them anyway to be absolutely certain everything is as it should be, or of course they would prove to be an invaluable starting point for investigations if you were to suffer more errors than you should.

As a guide as to what frequancy of errors can be expected you should note that correctly set up, in an office environment using good quality drives and diskettes, and with proper software, experience with several of these systems has been that they are error free. (Errors which are received, but which have a ready explanation, eg damaged diskettes, interrupted power supplies and so on, are of course not to be included here.)

Preliminaries

Before proceeding with the test of a new board, do the following:

1. Check that all components fitted so far are in the correct place, and have the correct polarity where appropriate. Re-read the constructional notes - important points are preceded by the loud word "Note!", and can be checked again now.

2. Inspect the board for dry joints, solder bridges and solder splashes, paying particular attention to areas where tracks run between IC pins. Shine a strong light through the board, and use a magnifying glass if you have one.

3. Apply power to the board and check that +5V is present and correct at all the IC sockets, i.e. at the upper right-hand corners of each. Beware particularly of damaging the IC socket connectors when probing them with test prods. If you consider you are likely to cause damage by carrying out this test, or are very confident of your previous workmanship, then omit this step at your own discretion.

4. Remove the power, and wait for the capacitors to discharge (if necessary use a few hundred ohm resistor to discharge them more quickly), and insert all ICs the correct way round.

   Usually the ICs are supplied with their leads slightly "splayed" - don't just shove them into their sockets; use the greatest care. An IC insertion tool will hold the leads parallel at the right spacing; if you don't have such a tool, bend the leads slightly at their "shoulder", on a flat surface. The sockets supplied in complete kits have been specially selected for their ability to provide high reliability connections, but the foregoing warnings are intensified if you are using your own sockets instead. There are some remarks in the Fault-finding Section later on the subject of difficulties which have been met with certain types of IC sockets, so study that before proceeding if you are in any doubt.

5. Important! Re-check the orientation and position of all ICs, as an error can have disastrous consequences. As it is hard to check your own work, preferably get someone else to check it for you.

6. Make the appropriate links on pin assemblies P1 to P19. Refer to Section 3.2 of this Manual for details. If you are not sure about any points, then ask your supplier for guidance. If this is not convenient then make a guess; any minor faults which occur due to a wrong guess can be rectified during further testing or when you gain actual operational experience with the board.

   Keep a note of the positions of all these links. The test procedures which follow will disturb many of them, so you will not want to go through the labour of working out all these details again. It is best to carry out the test procedures with

as many of the links in position as you can so that the results may be valid for actual operation; this is why the fitting of links has not been deferred until a later stage.

7. Set DIL switches S1a-S1e to suit the software in use. For Interak systems using Ports 80H onwards for the FDC-1 this is ON-OFF-OFF-OFF-OFF.

   Set DIL switches S1f-S1g to suit your personal preference and the software in use. Note that the use which is made of these switch settings depends entirely on the software in use, and the their functions may be totally different in any particular system.

Suggested switch selections in the absence of any other instructions:
S1f-h: OFF-OFF-OFF

8. Note that DIL switch S2a-h has no function at the time of writing. It can be set as follows:

   S2a-h: OFF-OFF-OFF-OFF-OFF-OFF-OFF-OFF

9. It is assumed that you have chamfered the connector edge of the board (this was instructed at step 4 of the constructional notes in section 3.1 of this manual; if you forgot to do it then do it now). Using a suitable contact lubricant (e.g. the "Evolube" proprietary product) apply a small quantity to the gold plated edge connector. This will greatly reduce wear on the gold plating and the bus sockets and will thus extend their useful life considerably.

   An alternative type of lubricant which has been used with no apparent ill effects is a branded product "Rocket WD-40"; however as it has extremely penetrating properties it should be used most sparingly to reduce the risk of lifting the gold-plated copper tracks which would render the card useless. Fit the card in such a position that you can adjust RV1-4 and CV1, and probe the various test-points, without removing the card, (preferably use an Interak Extender card, which can be purchased from your Interak supplier).

10. It has to be assumed at this stage that you have a working system with fully tested cards and a suitable monitor program. This is a safe enough assumption, as there would be little point in proceeding to add disks to a computer which was not working yet.

Compulsory Setting Up Procedures

The term compulsory need not be taken too literally. These procedures have to be followed if the card is to be brought up to its full designed standard, i.e. to suit all the main sizes of floppy disk, single and double sided, single and double density. Obviously if only single density is to be used there is no need to set up the part of

the card which deals with double density, and so on. However it is probably easier to do the full setting up for everything than it is to work out what can be left out, and the full setting up procedure is what is recommended.

Also, although the order of the procedures can be varied, it is recommended that they are done in the order given as this gives the clearest display on the oscilloscope (some of the later test pulses exhibit "jitter" if they are displayed before the voltage controlled oscillator has been set up).

General Remarks:

Suggestion, when carrying out tests: As most oscilloscopes are at best accurate to only a few percent and at worst can be widely out of adjustment, it is suggested that the 4 MHz crystal controlled signal at P5 pin 1 should be used to calibrate the oscilloscope, or better still all adjustments be made relative to this 4 MHz crystal frequency - for example when asked to set the voltage controlled oscillator to a frequency of 250 kHz note that this is exactly one-sixteenth of the 4 MHz frequency: with a steady hand on the trimmer, and a double trace oscilloscope it should be possible to display both signals simultaneously and confirm that sixteen cycles of the 4MHz signal do indeed fit into one cycle of the 250 kHz one.

Measurement Points: As the time intervals to be measured are quite short and the signals take a significant time to pass from a 1 to a 0 and vice versa there would be some doubt as to the correct settings if the voltage levels at which they are to be taken are not specified. For the purpose of what follows measure times from or to the moment a rising (0 going to 1) signal first passes through 2.4 volts, and a falling (1 going to 0) signal first passes through 0.45 volts.

Compulsory Test Number 1. Adjustment of VCO (Voltage Controlled Oscillator)

This is the setting of the voltage controlled oscillator centre frequency by varying CV1, the variable capacitor.

1. Ensure that the link on P11 is shorting pins 1 and 2 only, or is absent.

2. Operate the system reset switch (usually mounted on the CPU card front panel).

3. Put the FDC chip into test mode by moving the JLink to P11 pins 2 and 3. (If one of the JLinks supplied is a different colour or style from all the rest it should be used as the JLink for P11 to identify the "Test" function.)

   (Note: from now on do not operate the system reset switch as this action will disable the internal Voltage Controlled Oscillator (VCO) in the chip. If you do this accidentally, operation can be restored by removing the link on P11 pins 2 and 3 - or fitting it

to short pins 1 and 2 - and operating the system reset switch again, ie repeating steps 1 to 3 above.)

4. If you have a dual trace oscilloscope display the 4 MHz signal to be found at P5 pin 1 on one of the channels as a reference .

Observe the signal at P9 pin 2.

Instead of offering a long winded discussion of all the frequencies required of the voltage controlled oscillator for the various conditions of operation, the required results are summarised in the table below. (Four entries are shown in the table for completeness but in fact it is only strictly necessary to use one for setting up. The necessary alterations for different diameters and densities are carried out automatically within the chip, and there is thus no need to alter the variable capacitor for different diameters or densities. However if the controller card has never been used before you may care to verify all entries in the table just to make sure that it is indeed capable of coping with all the various formats correctly, ie all selection circuits are working correctly.)

Adjust the Variable capacitor (trimmer) CV1 as follows:

Data at Port 85	Diameter 5" or 8"	Density S/D or D/D	Required Frequency	ie Required Periodic Time
08	8"	D/D	500kHz	2us (2000ns)
0C	8"	S/D	250kHz	4us (4000ns)
00	5"	D/D	250kHz	4us (4000ns)
04	5"	S/D	125kHz	8us (8000ns)

(Note that the required frequency settings are exact factors of the 4 MHz signal used as a reference. Therefore, if a dual trace oscilloscope is available, by triggering from the signal at P9 pin 2, capacitor settings will be found which display both waveforms steadily; the correct setting can be confirmed by counting how many cycles of 4 MHz fit into just one cycle of the signal to be adjusted. In the four lines of the table above the factors for the frequencies 500kHz, 250kHz, 250kHz, and 125kHz, will be 8, 16, 16, 32 respectively.) If this technique is used, set the VCO trimmer CV1 in the middle of the very narrow range which will give a stable display.

Compulsory Test Number 2. Adjustment of Write Precompensation .

The floppy disk controller chip used has the ability to apply write precompensation when double density (MFM) recording is carried out. Precompensation counteracts the natural tendency (governed by the laws of magnetism) for the received data signals on the inner tracks to shift from their correct positions as the pattern of data recorded varies. The direction of the shift ("early" "nominal" or "late") can be predicted precisely according to the data pattern, and the FDC chip

alters the positions of the recorded data so that they will be correct when read later.

Often the manufacturers of 5" and smaller disk drives claim that no precompensation is necessary, but there is no real reason why the smaller diameter drives should be more isolated from the laws of magnetism than the 8" size: viewing the matter cynically it is more likely to be the case that the manufacturers have found the smaller drives sell better if this claim is made. Our own experience with this design is that good results are still obtained even if the write precompensation (for all diameter drives) is wildly out of specification, but this cannot be taken as a licence to ignore this adjustment - the provision of some write precompensation can never do any harm and will certainly do some good for any diameter drives if they are operated under adverse conditions (worn drives and diskettes, or in an electrically "noisy" environment, eg too close to sources of magnetic interference such as power supply transformers).

Note that the FDC chip applies no precompensation when single density (FM) recording is in operation. Nevertheless even if the system is never to be operated in double density we recommend for tidiness' sake that the precompensation adjustment be made.

5. (It is assumed that step 5 follows step 4 a page or two ago; if not you will have to carry out steps 1 to 3 before proceeding.)

   Observe the write pulse width at P9 pin 1. This is the amount of precompensation for use on the inner group of tracks for double density recording. The adjustment for 5" diskettes is made by varying RV1, and for 8" by RV2. The chip allows an adjustment range of at least 100ns to 300ns, typically 75ns to 550ns. The correct setting will be specified by the disk drive manufacturer, but 150ns and 200ns represent reasonable guesses for 5" and 8" respectively if you have to guess. Both RV1 and RV2 have to be adjusted, and the adjustment of each can be made independently, ie the setting of one does not disturb the other.

   The board has been laid out so that the direction of rotation of the adjustment screw is anticlockwise to reduce the setting, clockwise to increase it.

Data to Port 85	Diameter 5" or 8"	Potentiometer to Adjust	Example Setting
00 or 04	5"	RV1	150ns
08 or 0C	8"	RV2	200ns

Compulsory Test Number 3. Adjustment of Read Pulse Width

So that the floppy disk controller cand read data from the disk correctly adjustments are needed to set up the "data separator" part of the circuit and these are described next. This adjustment is compulsory in all circumstances.

6. If this step is not following those above you must first carry out steps 1, 2 and 3.

   Observe the signal at P9 pin 3. The correct waveform here will depend on the diameter of disk selected (5" or 8") and the recording format (single density or double density). The selection is made by outputting different data to Port 85, and the adjustment is made by varying the setting of RV3 for the 5" selections, and RV4 for the 8". As for the earlier adjustments, instead of offering a long winded discussion of the different settings required, the desired results are simply summarised in the table below. (Four entries are shown in the table for completeness but in fact it is only strictly necessary to use two - one for 5" and one for 8" - because the necessary alteration between single and double density takes place automatically within the chip; the setting of each variable resistor does not need to change when changing the recording density on a given diameter of disk.)

   The board has been laid out so that an anticlockwise adjustment of the potentiometers reduces the pulsewidth and a clockwise adjustment increases it.

   A small amount of jitter (say 50ns) may be accepted in these waveforms; if so make the adjustment so that the average pulsewidth observed is equal to the value given below under the heading "Required Pulsewidth"

Data to Port 85	Diameter 5" or 8"	Density S/D or D/D	Repetition Rate (time)	Required Pulsewidth	Potentiometer to Adjust
00	5"	D/D	250kHz (4us)	500ns	RV3
04	5"	S/D	125kHz (8us)	1000ns	RV3
08	8"	D/D	500kHz (2us)	250ns	RV4
0C	8"	S/D	250kHz (4us)	500ns	RV4

Finally:

7. Important! Don't forget to do this! (The board will not work if it is left in test mode, and many futile hours of fault-finding may result): Restore normal operation by removing the JLink shorting P11 pins 2 and 3, and operating the system reset. If desired the JLink can be "parked" shorting P11 pins 1 and 2.

This completes the Compulsory Setting Up procedures. The Optional ones begin on the next page.

Optional Test Sequence 1.

1. Link P8 1-2 (and leave this link throughout). Press Reset or using your system monitor (ZYMON 2 or whatever you have instead) Output to Port 85 data 00, i.e. select 5" D/D

   Probe Pin Assembly P5, using an oscilloscope.

   P5 Pin 1 f = 4.00 MHz; T = 250 ns
   P5 Pin 2 f = 2.00 MHz; T = 500 ns
   P5 Pin 3 f = 1.00 MHz; T = 1000 ns, i.e. 1 us
   P5 Pin 4 Logic "1"

2. Output to Port 85 data 04, i.e. 5" S/D

   As for 1 above, namely:

   P5 Pin 1 f = 4.00 MHz; T = 250 ns
   P5 Pin 2 f = 2.00 MHz; T = 500 ns
   P5 Pin 3 f = 1.00 MHz; T = 1000 ns, i.e. 1 us
   P5 Pin 4 Logic "1"

3. Output to Port 85 data 08, i.e. 8" D/D

   P5 Pin 1 f = 4.00 MHz; T = 250 ns
   P5 Pin 2 Logic "1"
   P5 Pin 3 f = 2.00 MHz; T = 500 ns
   P5 Pin 4 Logic "0"

4. Output to Port 85 data 0C, i.e. 8" S/D

   As for 3 above, namely:

   P5 Pin 1 f = 4.00 MHz; T = 250 ns
   P5 Pin 2 Logic "1"
   P5 Pin 3 f = 2.00 MHz; T = 500 ns
   P5 Pin 4 Logic "0"

Optional Test Sequence 2.

1. Link P6 pins 2-3 only. (This allows U9 to be permanently enabled, regardless of the state of the signal at U1 pin 12.)

   Output the following data to Port 85 and confirm that the following outputs are found at the pins of U9:

Data @ Port 85	U9 Pin 12	U9 Pin 11	U9 Pin 10	U9 Pin 9
00	1	1	1	0
01	1	1	0	1
02	1	0	1	1
03	0	1	1	1
20	1	1	1	1

Link P6 pins 1-2 only (This allows the output, U1 pin 12, of the "motors on" monostable to disable all the outputs from U9 after a time which is selected by the links on P5 and P2.)

Confirm that immediately after outputting to Port 85 the data shown in the first four lines of the above table, that the "0"s in the right hand side of the table persist only for a limited time (around 5 to 15 seconds, according to the particular settings on P1 and P6). Change the settings on P1 and P2, and confirm that the time varies. Typical results are given below for C1, C2, C3 all 47uF, and R1 220k:

P1	P2	Typical "Motors On" Time
1-2	1-2	12 seconds (nominal 15 sec)
1-2	2-3	8 seconds (nominal 10 sec)
2-3	1-2	8 seconds (nominal 10 sec)
2-3	2-3	4 seconds (nominal 5 sec)

Leave P1, P2, P6 set at whatever suits your requirements for the system in use.

Optional Test Sequence 3.

Set S1f, S1g, S1h, all "on". Link P12 pins 2-3. Use your system monitor to input data from port 85, and confirm that it agrees with that shown in the first line of the following table. Then repeat the test with different settings of S1f, S1g, S1h, and the link on P12, and confirm that the correct results are obtained. In the table below "X" means the data is unknown; typically "X" appears as "F" in a standard implementation of this card.

S1f	S1g	S1h	P12	Data Input from Port 85
ON	ON	ON	2-3	0X
ON	OFF	ON	No Link	5X
OFF	ON	OFF	2-3	AX
OFF	OFF	OFF	No link	FX

Next set up the following conditions:

S1f	S1g	S1h	P12	Data Input from Port 85
ON	ON	ON	1-2	See next paragraph

Check that the data found when inputting from Port 85 under these conditions is as follows:

After the system has been left for a little while (say half a minute) an input from Port 85 (use your monitor's port input command), without a prior output to that port should result in

data of 1X. (Again "X" is any data; typically this appears as "F".)

Immediately after an output instruction to Port 85 (use your monitor's port output command) the input data from Port 85 is 0X.

About 5-15 seconds later (depending on the settings on P1 and P2) it reverts to 1X, and remains like that until a further output command to Port 85.

Leave S1f-h and P12 set to suit the requirements for the system in use.

Optional Test Sequence 4.

Set S2a-S2h (8 switches) all "on". Use your system monitor to input data from port 86, and confirm that it agrees with that shown in the first line of the following table. Then repeat the test with different settings of S2a-S2h and confirm that the other results are obtained.

S2a	S2b	S2c	S2d	S2e	S2f	S2g	S2h	Data Input from Port 85
ON	ON	ON	ON	ON	ON	ON	ON	00
ON	OFF	ON	OFF	ON	OFF	ON	OFF	55
OFF	ON	OFF	ON	OFF	ON	OFF	ON	AA
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	FF

Leave S2a-h at whatever your system requires (all off if this is not specified).

Optional Test Sequence 5.

This is to test the "Artificial Ready" part of the monostable U1, type 74LS123. Normally this is triggered from the index pulses received from the selected disk drive, but for testing a temporary arrangement is now described to allow the monostable to be triggered from the system reset line.

Connect DH2 pins 1-6 by any suitable means.

Remove the JLink on pin assembly P3.

Probe P3 pin 1, and confirm the following results:

When P3 pins 2-3 are linked P3 pin 1 should be "0" (low).
When no links are made on P3 its pin 1 should be "1" (high).

Leave P3 temporarily with no links fitted, and connect by any suitable means DH2 pin 12 to pin 1 of U23, the 74LS132.

Set up the oscilloscope so that it triggers reliably on negative edges of an input signal. A convenient signal which can be used

for this is to be found at say P5 pin 1. Now alter the timebase of the oscilloscope if necessary so that negative pulses of width about 350 ms can be displayed.

Probe P3 pin 1.

Confirm that a negative going pulse of duration approximately 350 ms ± 50% is generated at P3 pin 1 whenever the system reset is activated.

Remove all of the test connections and replace the JLink in the appropriate position on P3 (usually this is to link 1-2).

Optional Test Sequence 6.

This is to test the "Head Load" part of the monostable U21, type 74LS123. Normally this is triggered from the head load output from the floppy disk chip itself (U11 pin 23) , but for testing a temporary arrangement is now described to allow the monostable to be triggered from the system reset line.

Set up the oscilloscope so that it triggers reliably on negative edges of an input signal. A convenient signal which can be used for this is to be found at say P5 pin 1. Now alter the timebase of the oscilloscope if necessary so that negative pulses of width up to 100 ms can be displayed.

Remove U14 (a 74LS244) from its socket.
Connect DH2 pins 1-6 by any suitable means.

Connect by any suitable means U23 (74LS132) pin 1, to U20 (7406) pin 1.

Set up the oscilloscope so that it triggers reliably on negative edges of an input signal. A convenient signal which can be used for this is to be found at say P5 pin 1. Now alter the timebase of the oscilloscope if necessary so that negative pulses of width about 350 ms can be displayed.

Probe U11 (the FDC chip) pin 40.

Confirm that a negative going pulse of duration in the range 30ms-100ms (approximately) is generated at U11 pin 40 whenever the system reset switch is operated.

Change the positions of the JLinks on P13 and P14 and check that the duration of the pulse varies in accordance with the following table:

P13	P14	Equivalent Timing Resistor	Head Load Time Calculated	Typical
1-2	1-2	8.2k	37 ms	30 ms
1-2	2-3, (or none)	11k	50 ms	40 ms
2-3, (or none)	1-2	13k	60 ms	50 ms
2-3, (or none)	2-3, (or none	22k	100 ms	80 ms

If the results are wildly out, say by 20% or more, and assuming no circuit fault or defective components R20,21,22, U21, C25, then they can be brought into line by altering the value of C25. Increasing the value of C25 will increase the pulsewidth, and vice versa. Note that there is a vacant position, C24, on the board which can be used to add further capacitance if C25 is judged to be low, to save removing C25 itself. If C25 needs to be replaced and C24 is not fitted yet, then to save desoldering damage on the board C25 can be cut out with wire cutters and the replacement soldered in position C24.

(Note that all of these head load monostable adjustment facilities are far more extensive than are given in an average design, so if they seem too complicated you are justified in ignoring them and hoping for the best - the performance then will be no worse than popular home computers which have sold in their millions with total disregard to the niceties of design aspects like this. Even with a grossly inadequate head load time setting the FDC chip's own error detecting facilities will protect the user's data by causing a "retry" which will usually be totally undetectable by the user.)

Remove all of the test connections and leave the JLinks in the appropriate positions on P13 and P14.

Optional Test Sequence 7.

This sequence is to prove that the "Enable Precompensation" circuits are working correctly.

Link P8 1-2 throughout these tests (and generally throughout all normal operation).

Operate the system reset switch.

Remove the JLink on P17.

Probe the FDC chip U11, pin 1; this should be a "1" (high) with no links on P17, and should be "0" (low) when P17 pins 2-3 are linked.

Fit no JLink on P17 and link P18 2-3. Probe P17 pin 1 for the rest of the tests.

Output to Port 85H (use your monitor's Port command) any data which has a "0" as bit 4, eg data 00H. Confirm P17 pin 1 is "0"

(low).

Output to Port 85H any data which has a "1" as bit 4, eg data 10H. Confirm P17 pin 1 is "1" (high).

Link P18 1-2.

Put the FDC chip U11 into test mode by following the sequence:

1. Ensure that the link on P11 is shorting pins 1 and 2 only, or is absent.

2. Operate the system reset switch (usually mounted on the CPU card front panel).

3. Put the FDC chip into test mode by moving the JLink to P11 pins 2 and 3. (If one of the JLinks supplied is a different colour or style from all the rest it should be used as the JLink for P11 to identify the "Test" function.)

(Note: from now on do not operate the system reset switch as this action will disable the internal Voltage Controlled Oscillator (VCO) in the chip. If you do this accidentally, operation can be restored by removing the link on P11 pins 2 and 3 - or fitting it to short pins 1 and 2 - and operating the system reset switch again, ie repeating steps 1 to 3 above.)

Output to Port 85 data 00H.

Link P19 1-2; confirm P17 pin 1 is "0" (low).

Link P19 2-3; confirm P17 pin 1 now carries a train of short positive pulses. (If RV3 has been adjusted these will be of width 500ns, repeated at 4 us intervals; if not you can alter RV3 if you wish. For the present purposes we so not care about the dimensions of the signal; we are only checking the logic paths are open for the ENP signal which will be present when the FDC chip is operated normally, out of test mode.)

No Link on P19. Confirm the same pulse train as described above is present on P17 pin 1.

Link P19 3-4. Confirm the same pulse train as described above is present on P17 pin 1.

Output to Port 85 data 0CH.

The comments and results above for when the data was 00H apply again, with the one exception that it is now the setting of RV4 which determines the pulse width. Leave RV4 alone if it has already been set, if not you may alter it. Check the set of results as given above, ie P19 1-2, P19 2-3, P19 No Link, P19 3-4.

Remove the probe from P17 pin 1 and replace the appropriate

JLinks on P17, P18, P19. (Typically P17 1-2, P18 1-2, P19 2-3.)

Important: If no further testing is to be carried out, the FDC chip must be taken out of test mode: restore normal operation by removing the JLink shorting P11 pins 2 and 3, and operating the system reset. If desired the JLink can be "parked" shorting P11 pins 1 and 2.

This concludes testing and setting up. The next section of the Manual covers fault finding, and return for service.

FDC-1 PORT ALLOCATIONS

Port No. used in Interak 1	FDC Chip Select	READ (NRDS=0)	WRITE (NWDS=0)
80H	0	FDC Chip Status Register "DSTATUS" (8 Bits)	FDC Chip Command Register "DCOMM" (8 Bits)
81H	0	FDC Chip Track Register "DTRACK" (8 Bits)	FDC Chip Track Register "DTRACK" (8 Bits)
82H	0	FDC Chip Sector Register "DSECTOR" (8 Bits)	FDC Chip Sector Register "DSECTOR" (8 Bits)
83H	0	FDC Chip Data Register "DDATA" (8 Bits)	FDC Chip Data Register "DDATA" (8 Bits)
84H	1	Disk Polling. "DPOLL" Bit 0 INTRQ 1 Logic 0 2 Logic 0 3 Logic 0 4 Logic 0 5 Logic 0 6 Logic 0 7 DRQ	Not Used Port decoded, but not used
85H	1	Disk Configuration "DCONR" Bit 0 2 Sided Diskette (L) 1 Spare 1 (L) 2 Spare 2 (L) 3 Spare 3 (L) 4 Motor Mono Status (L) 5 *Unallocated (S1h) 6 *Unallocated (S1g) 7 *Unallocated (S1f)	Disk Configuration "DCONW" Bit 0 1 0,1,2,3 (= A,B,C,D) 2 Single Density (H) 3 Select 8" (H) 4 Enable Precomp (H) 5 Deselect All (H) 6 Motors On (H) 7 Lock Doors (H)
86H	1	Disk Option Sw. "DOPTS" Bit 0 *Unallocated (S2h) 1 *Unallocated (S2g) 2 *Unallocated (S2f) 3 *Unallocated (S2e) 4 *Unallocated (S2d) 5 *Unallocated (S2c) 6 *Unallocated (S2b) 7 *Unallocated (S2a)	Not Used Port decoded, but not used
87H	1	Port decoded, but not used	Port decoded, but not used

*Function depends on software in use

Interak Standard Interface Connector for 8" Drives

The interface connector used on most current 8" drives is a 50-way double sided 0.1" pitch card-edge type. A 50-way ribbon (or 25 twisted pair) cable conveys the signals between the drive(s) and the FDC-1 card. The connector (J1) on the FDC-1 card is a 50-way ribbon cable header with pins numbered as in the tables which follow. The FDC-1 uses only those signals which are almost certain to be found on a given "industry standard" 8-inch disk drive; the functions of the unused lines are often different from one manufacturer to another, so cannot be fully specified here.

For your convenience, the table is given twice, initially with the pins numbered in the normal ascending order, and then in reverse order - because this is the way they appear physically on the FDC-1 card and on the circuit diagram (diagram sheet 2). The second table will be the more useful if you are trying to work out some special links for yourself.

Table of Interak Standard 8" (50-way) connections, in ascending order.

J1 Pin No.		Dir	Signal Name	Signal No.	
	2	[OUT]	Track 43 (L)	1	Gnd, 0V
	4	[IN]	Spare 1 (Not used by FDC1)	3	Gnd, 0V
	6	[IN]	Spare 2 (Not used by FDC1)	5	Gnd, 0V
	8	[IN]	Spare 3 (Not used by FDC1)	7	Gnd, 0V
	10	[IN]	2-Sided Diskette (L)	9	Gnd, 0V
	12	[IN]	Disk Change (Not used by FDC1)	11	Gnd, 0V
	14	[OUT]	Side 1 Select (L)	13	Gnd, 0V
	16	[OUT]	Lock Door/In Use (L)	15	Gnd, 0V
(2)	18	[OUT]	Head Load (L)	(1) 17	Gnd, 0V
(4)	20	[IN]	Index (L)	(3) 19	Gnd, 0V
(6)	22	[IN]	Ready (L)	(5) 21	Gnd, 0V
(8)	24	[IN]	- (Not used by FDC-1)	(7) 23	Gnd, 0V
(10)	26	[OUT]	Drive Select 0 "A" (L)	(9) 25	Gnd, 0V
(12)	28	[OUT]	Drive Select 1 "B" (L)	(11) 27	Gnd, 0V
(14)	30	[OUT]	Drive Select 2 "C" (L)	(13) 29	Gnd, 0V
(16)	32	[OUT]	Drive Select 3 "D" (L)	(15) 31	Gnd, 0V
(18)	34	[OUT]	Direction In (L)	(17) 33	Gnd, 0V
(20)	36	[OUT]	Step (L)	(19) 35	Gnd, 0V
(22)	38	[OUT]	Write Data (L)	(21) 37	Gnd, 0V
(24)	40	[OUT]	Write Gate (L)	(23) 39	Gnd, 0V
(26)	42	[IN]	Track 00 (L)	(25) 41	Gnd, 0V
(28)	44	[IN]	Write Protected (L)	(27) 43	Gnd, 0V
(30)	46	[IN]	Read Data (L)	(29) 45	Gnd, 0V
(32)	48	[IN]	- (Not used by FDC-1)	(31) 47	Gnd, 0V
(34)	50	[IN]	- (Not used by FDC-1)	(33) 49	Gnd, 0V

For the same table repeated with the pins numbered in descending order and the notes on both tables, see the next page.

Table of Interak Standard 8" (50-way) connections, in descending order.

J1 Pin No.		Dir	Signal Name	Signal No.		Signal Name
(34)	50	[IN]	- (Not used by FDC-1)	(33)	49	Gnd, 0V
(32)	48	[IN]	- (Not used by FDC-1)	(31)	47	Gnd, 0V
(30)	46	[IN]	Read Data (L)	(29)	45	Gnd, 0V
(28)	44	[IN]	Write Protected (L)	(27)	43	Gnd, 0V
(26)	42	[IN]	Track 00 (L)	(25)	41	Gnd, 0V
(24)	40	[OUT]	Write Gate (L)	(23)	39	Gnd, 0V
(22)	38	[OUT]	Write Data (L)	(21)	37	Gnd, 0V
(20)	36	[OUT]	Step (L)	(19)	35	Gnd, 0V
(18)	34	[OUT]	Direction In (L)	(17)	33	Gnd, 0V
(16)	32	[OUT]	Drive Select 3 "D" (L)	(15)	31	Gnd, 0V
(14)	30	[OUT]	Drive Select 2 "C" (L)	(13)	29	Gnd, 0V
(12)	28	[OUT]	Drive Select 1 "B" (L)	(11)	27	Gnd, 0V
(10)	26	[OUT]	Drive Select 0 "A" (L)	(9)	25	Gnd, 0V
(8)	24	[IN]	- (Not used by FDC-1)	(7)	23	Gnd, 0V
(6)	22	[IN]	Ready (L)	(5)	21	Gnd, 0V
(4)	20	[IN]	Index (L)	(3)	19	Gnd, 0V
(2)	18	[OUT]	Head Load (L)	(1)	17	Gnd, 0V
	16	[OUT]	Lock Door/In Use (L)		15	Gnd, 0V
	14	[OUT]	Side 1 Select (L)		13	Gnd, 0V
	12	[IN]	Disk Change (Not used by FDC1)		11	Gnd, 0V
	10	[IN]	2-Sided Diskette (L)		9	Gnd, 0V
	8	[IN]	Spare 3 (Not used by FDC1)		7	Gnd, 0V
	6	[IN]	Spare 2 (Not used by FDC1)		5	Gnd, 0V
	4	[IN]	Spare 1 (Not used by FDC1)		3	Gnd, 0V
	2	[OUT]	Track 43 (L)		1	Gnd, 0V

Notes on last two tables.

The numbers in brackets are the corresponding ribbon cable conductor numbers if a 34-way ribbon cable (for smaller drives) is fitted in place of the 50-way cable used for 8" drives.

The legend (L) means that the named signal goes to a logic "0" (ie approaches 0V) to fulfil its purpose. The direction of the signal, as given in the "Dir" column, is specified from the point of view of the computer, eg, a signal which comes out of the disk drive and into the FDC-1 interface is shown as [IN].

So far we have listed the signals on J1 for the 50-way interface signals for the 8" diameter disk drives. The next few pages describe the 34-way ribbon cable interface signals on connector J1 for smaller (3", 3.5", 5.25") drives, and after that we will discuss the links to be made on DIL Headers DH2 and DH3, to correspond to the "Interak Standard" 50-way and 34-way interfaces described in the tables.

Interak Standard Interface Connector for non-8" Drives

Disk drives smaller than 8" use a 34-way ribbon cable. There are two types of connector used where the cable mates with the drive; generally for 5.25" drives a double sided 0.1" pitch card-edge connector is used and for the 3.5" size a ribbon cable header type. On 3" drives it is anybody's guess, but will probably be one of these two. A 34-way ribbon (or 17 twisted pair) cable conveys the signals between the drive(s) and the FDC-1 card. We specify that regardless of whether the cable is 34-way or 50-way, the connector (J1) at the FDC-1 end of the interface cable is always a 50-way type. This is so that different types of drives can be used without the need to change J1 on the FDC-1 card.

When the 34-way cable is terminated in the 50-way connector, it should be installed in such a way that the conductors numbered 1-34 will correspond to conductors numbered 18-50 for the 50-way cable.

As before for the 8" signals, the table is given twice, initially with the pins numbered in the normal ascending order, and then in reverse order - because this is the way they appear physically on the FDC-1 card and on the circuit diagram (diagram sheet 2). The second table will be the more useful if you are trying to work out some special links for yourself.

Table of Interak Standard non-8" (34-way) connections, in ascending order.

Signal No.		Dir	Signal Name	Signal No.		Signal Name
(2)	18	-	(Not used by FDC-1)	(1)	17	Gnd, 0V
(4)	20	[OUT]	Head Load/In Use (L)	(3)	19	Gnd, 0V
(6)	22	[OUT]	Drive Select 3 "D" (L)	(5)	21	Gnd, 0V
(8)	24	[IN]	Index	(7)	23	Gnd, 0V
(10)	26	[OUT]	Drive Select 0 "A" (L)	(9)	25	Gnd, 0V
(12)	28	[OUT]	Drive Select 1 "B" (L)	(11)	27	Gnd, 0V
(14)	30	[OUT]	Drive Select 2 "C" (L)	(13)	29	Gnd, 0V
(16)	32	[OUT]	Motor On (L)	(15)	31	Gnd, 0V
(18)	34	[OUT]	Direction In (L)	(17)	33	Gnd, 0V
(20)	36	[OUT]	Step (L)	(19)	35	Gnd, 0V
(22)	38	[OUT]	Write Data (L)	(21)	37	Gnd, 0V
(24)	40	[OUT]	Write Gate (L)	(23)	39	Gnd, 0V
(26)	42	[IN]	Track 00 (L)	(25)	41	Gnd, 0V
(28)	44	[IN]	Write Protected (L)	(27)	43	Gnd, 0V
(30)	46	[IN]	Read Data (L)	(29)	45	Gnd, 0V
(32)	48	[OUT]	Side 1 Select (L)	(31)	47	Gnd, 0V
(34)	50	[IN]	Ready (L)	(33)	49	Gnd, 0V

For the same table repeated in descending order and the notes on both tables, see the next page.

Table of Interak Standard non-8" (34-way) connections, in descending corder.

J1 Pin No.		Dir	Signal Name	Signal No.		Signal Name
(34)	50	[IN]	Ready (L)	(33)	49	Gnd, 0V
(32)	48	[OUT]	Side 1 Select (L)	(31)	47	Gnd, 0V
(30)	46	[IN]	Read Data (L)	(29)	45	Gnd, 0V
(28)	44	[IN]	Write Protected (L)	(27)	43	Gnd, 0V
(26)	42	[IN]	Track 00 (L)	(25)	41	Gnd, 0V
(24)	40	[OUT]	Write Gate (L)	(23)	39	Gnd, 0V
(22)	38	[OUT]	Write Data (L)	(21)	37	Gnd, 0V
(20)	36	[OUT]	Step (L)	(19)	35	Gnd, 0V
(18)	34	[OUT]	Direction In (L)	(17)	33	Gnd, 0V
(16)	32	[OUT]	Motor On (L)	(15)	31	Gnd, 0V
(14)	30	[OUT]	Drive Select 2 "C" (L)	(13)	29	Gnd, 0V
(12)	28	[OUT]	Drive Select 1 "B" (L)	(11)	27	Gnd, 0V
(10)	26	[OUT]	Drive Select 0 "A" (L)	(9)	25	Gnd, 0V
(8)	24	[IN]	Index	(7)	23	Gnd, 0V
(6)	22	[OUT]	Drive Select 3 "D" (L)	(5)	21	Gnd, 0V
(4)	20	[OUT]	Head Load/In Use (L)	(3)	19	Gnd, 0V
(2)	18	-	(Not used by FDC-1)	(1)	17	Gnd, 0V

Notes on the last two tables

The numbers in brackets are the corresponding ribbon cable conductor numbers for the 34-way cable.

The legend (L) means that the named signal goes to a logic "0" (ie approaches 0V) to fulfil its purpose. The direction of the signal, as given in the "Dir" column, is specified from the point of view of the computer, eg, a signal which comes out of the disk drive and into the FDC-1 interface is shown as [IN].

Unlike those for the 3.5" and 8" sizes of drives, the signals used for 3" and 5.25" can vary quite considerably from one manufacturer to another. The signals on J1 even numbered pins 24 to 46 inclusive (ie ribbon cable conductors 8 to 30) are the same for virtually all non-8" drives, but those on J1 pins 18, 20, 22, 48 and 50 (ie ribbon cable numbers 2, 4, 6, 32, 34) can vary depending on the model of drive connected. In the design of the FDC-1 we hope that we have caught most of the common variations, so that it should be possible to find a suitable set of links on the DIL headers DH2 and DH3 to cover most drives. The 3" drives are now so rare that it is we can only guess as to what their standard should be, but we believe that they mostly conform to the allocations given in the tables above.

Links to be Made on DIL Headers DH2 and DH3

These two DIL headers have been provided so that (we hope) you will be able to make the interface signals correspond with those that you require to suit your drives. This should be quite easy if you have modern drives which are very likely to correspond to what we have defined in the last few pages as the "Interak Standard Disk Drive Interfaces". It is a simple matter of deciding if the signals correspond to the 8" standard or the non-8" standard; sometimes disk drive manufacturers do as we do and allow you to scramble some of the signals, so that you can fit in with other equipment, and if this is the case we suggest that you stick to the standards we have defined and make both the drives and the interface signals comply. However you may find your drive is non-standard in a few respects, and cannot be made to conform; in this case the ability to alter the interface by making alternative connections on the FDC-1 card DIL headers may save the day.

A far more technical problem to solve has to be faced if you want to run a mixture of incompatible drives from the same interface. No specific guidance can be given on this point as each case has to be considered on its merits, but possible solutions could be external scrambling of the connections in the form of a "bump in the cable", perhaps passively, just by interchanging wires, or actively via integrated circuit multiplexers (eg the 74LS257 1-line to 2-line multiplexer for 2 different drives, or the 74LS253 1-line to 4-line multiplexer for 3 or 4 different drives), with duplicated drivers for outputs and terminating networks for receivers. In the active arrangement a convenient place to install all this paraphernalia is on a board which plugs into the rack - one cable comes in from the FDC-1 card and, one or more cables come out to your own weird and wonderful special disk drives. Note that the circumstances considered in this paragaph are extremely abnormal, and no recommended Interak system would involve this complication.

However, back to the simple life. Below are presented the two groups of connections which are to be made on DIL headers DH2 and DH3 to suit the two main standards: 8" (50-way) and non-8" (34-way). Don't forget, if you think all of these options on the FDC-1 are an inconvenience, that you don't have to use them if you don't want to. If you wish that you had a simple home computer, where all you get is one disk socket with a pre-ordained set of signal allocations, then this is easily arranged on the FDC-1, by fitting the links below for the non-8" (34-way) case.

(Diagrams printed on next page so that they need not be split)

Links on DIL Headers DH2, DH3

(a) For the 8" (50-way) Interface

DH2 (8")

```
1      16
2      15
3      14
4      13
5      12
6      11
7      10
8       9
```

(Fit no links)

(b) For the non-8" (34-way) Interface

DH2 (non-8")

```
1      16
2-----15   Ready (L)
3      14
4      13
5-----12   Side 1 Select (L)
6-----11   Motor On (L)
7-----10   Head Load (L)
8       9
```

(Fit 4 links)

(If your drive has no "Ready" signal, then delete link 2-15 above, and use instead the "Artificial Ready", by making link 1-16.)

DH3 (8")

```
1-----16   Drive Select 3 (L)
2      15
3-----14   Ready (L)
4      13
5-----12   Index (L)
6      11
7-----10   Head Load (L)
8       9
```

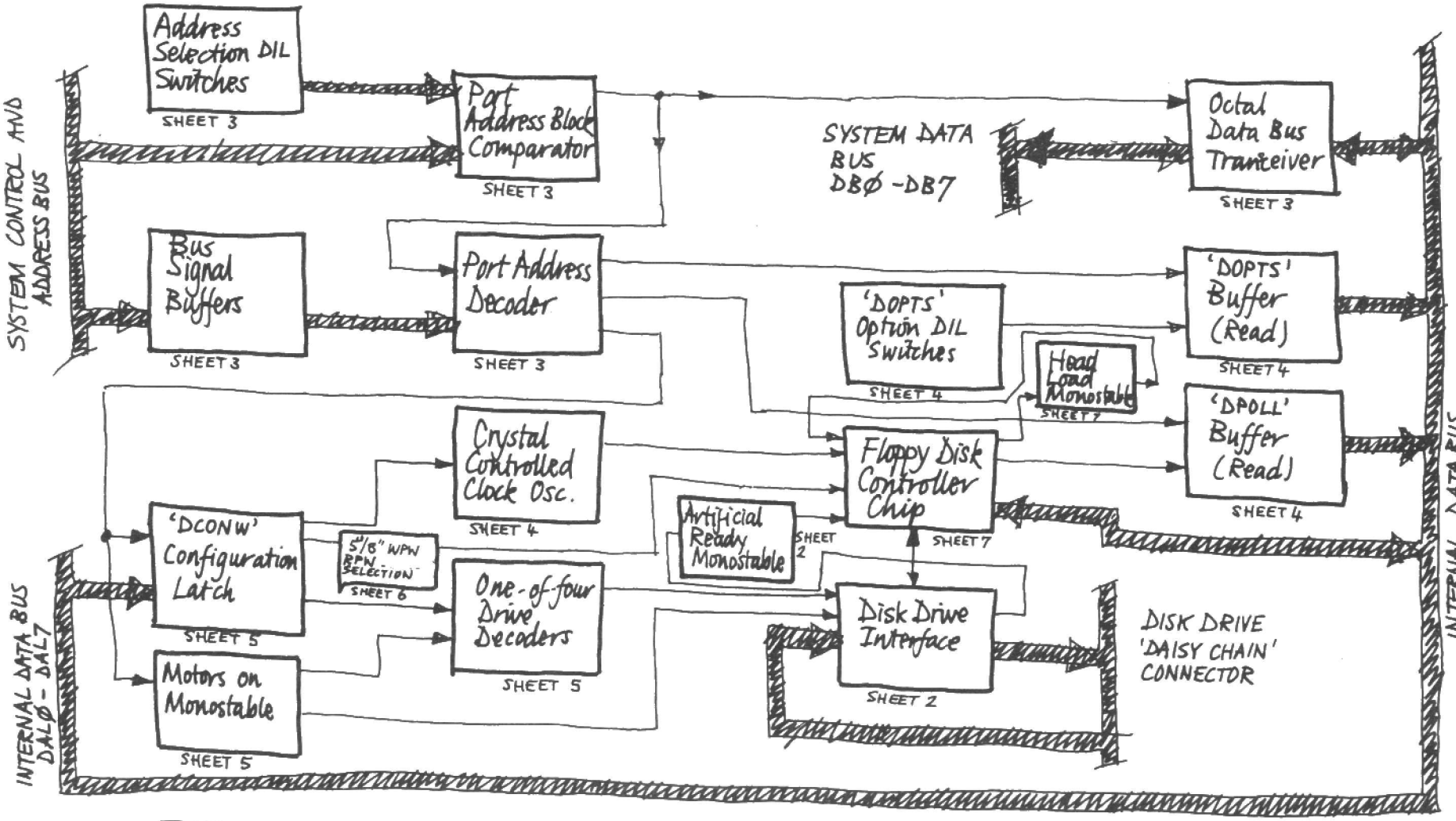
(Fit 4 links)

DH3 (non-8")

```
1      16
2-----15   Index (L)
3      14
4-----13   Drive Select 3 (L)
5      12
6      11
7      10
8       9
```

(Fit 2 links)

This concludes the present discussion of the interface signal allocations and the corresponding links to be made on the DIL headers DH2 and DH3.

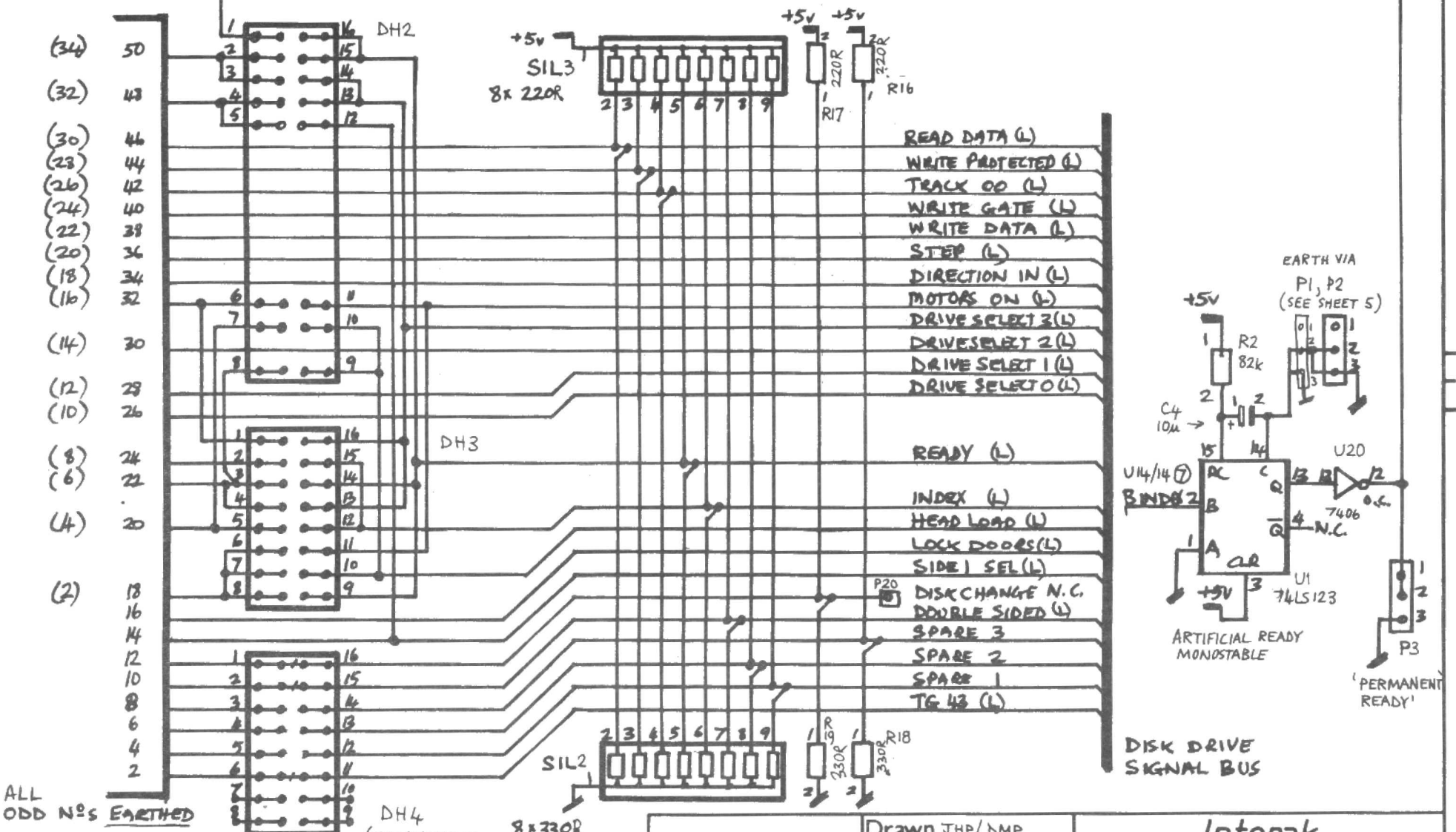


Drawn	DMP
Date	6-6-85
Scale	–

Greenbank Electronics

FDC-1 CIRCUIT DIAGRAM SHEET 1: BLOCK DIAGRAM

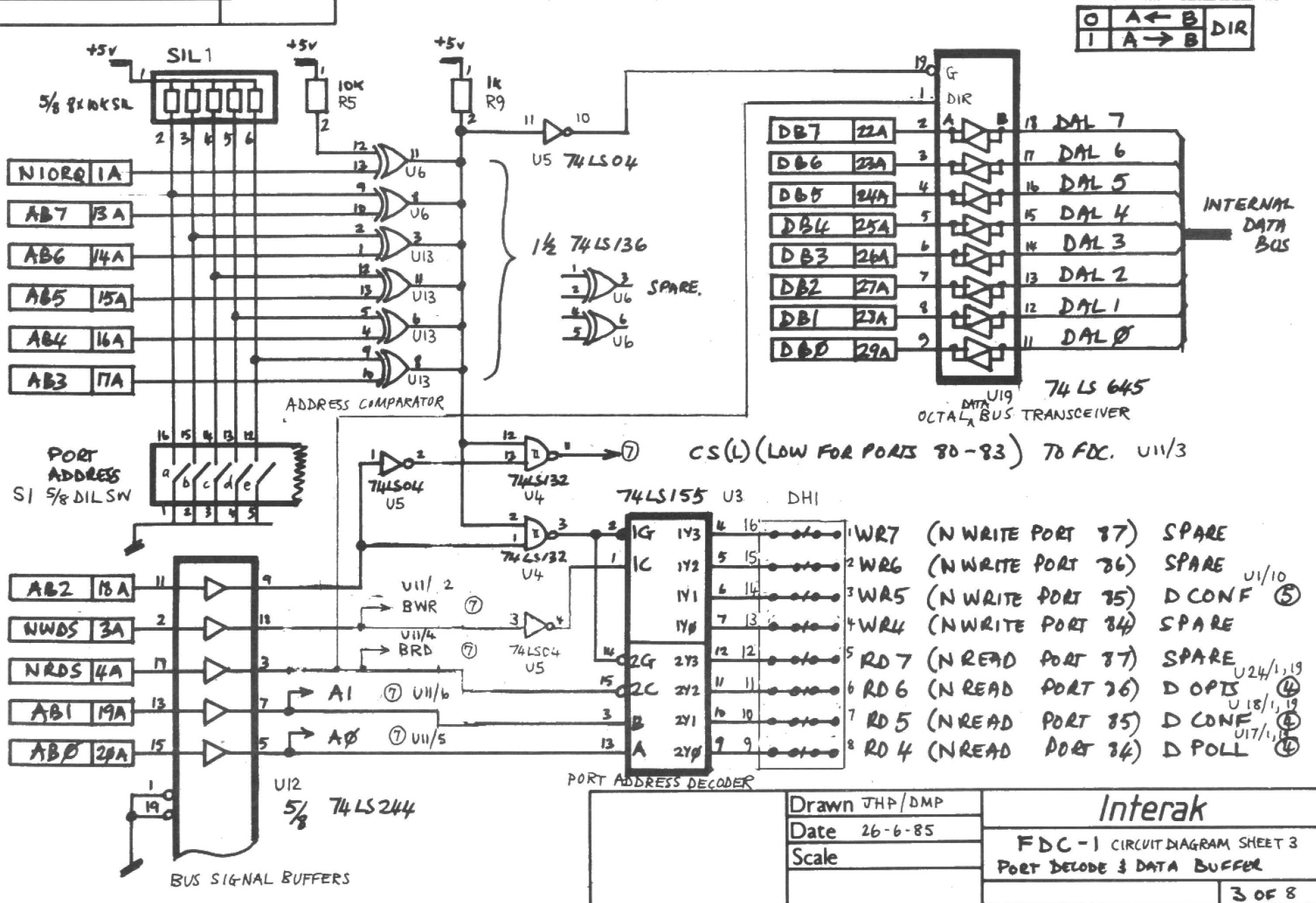
1 OF 8



Drawn	JHP/DMP
Date	6-6-85
Scale	-

Interak

FDC-1 CIRCUIT DIAGRAM SHEET 2:
DISK DRIVE SIGNAL BUS

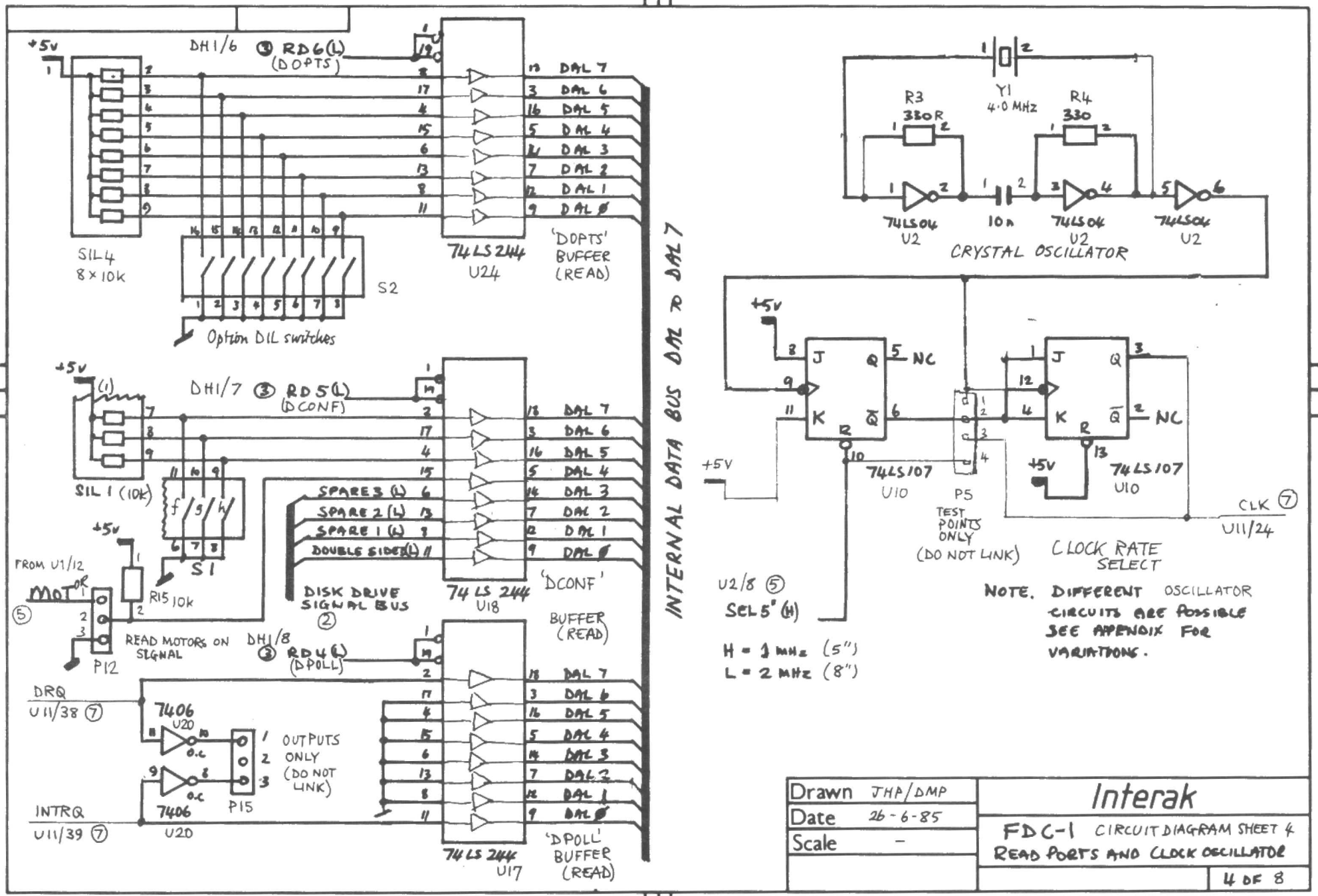


Drawn	JHP/DMP
Date	26-6-85
Scale	

Interak

FDC-1 CIRCUIT DIAGRAM SHEET 3
PORT DECODE & DATA BUFFER

3 OF 8

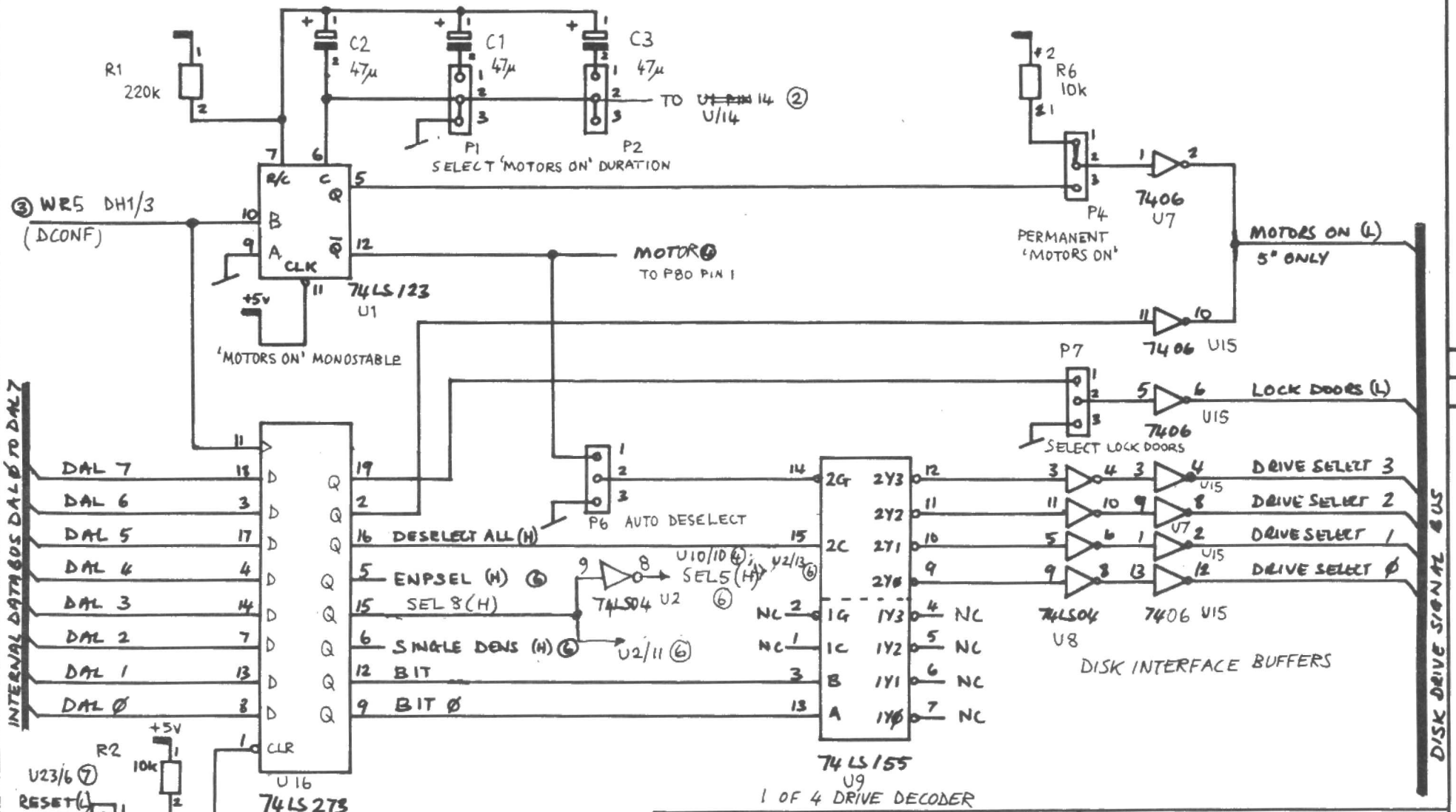


Drawn	JHP/DMP
Date	26-6-85
Scale	–

Interak

FDC-1 CIRCUIT DIAGRAM SHEET 4
READ PORTS AND CLOCK OSCILLATOR

4 OF 8

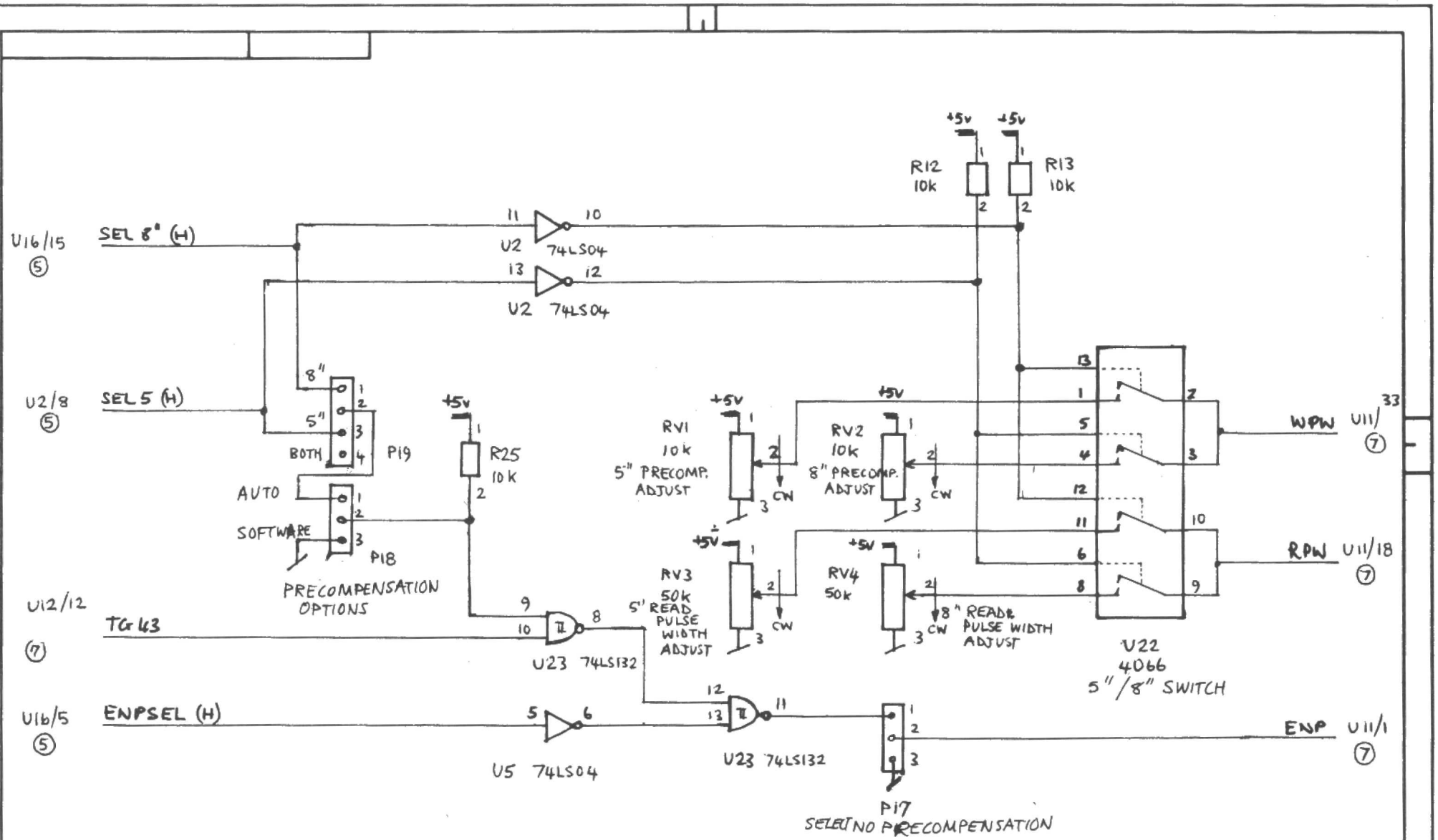


Drawn	JHP/DMP
Date	26-6-85
Scale	-

Interak

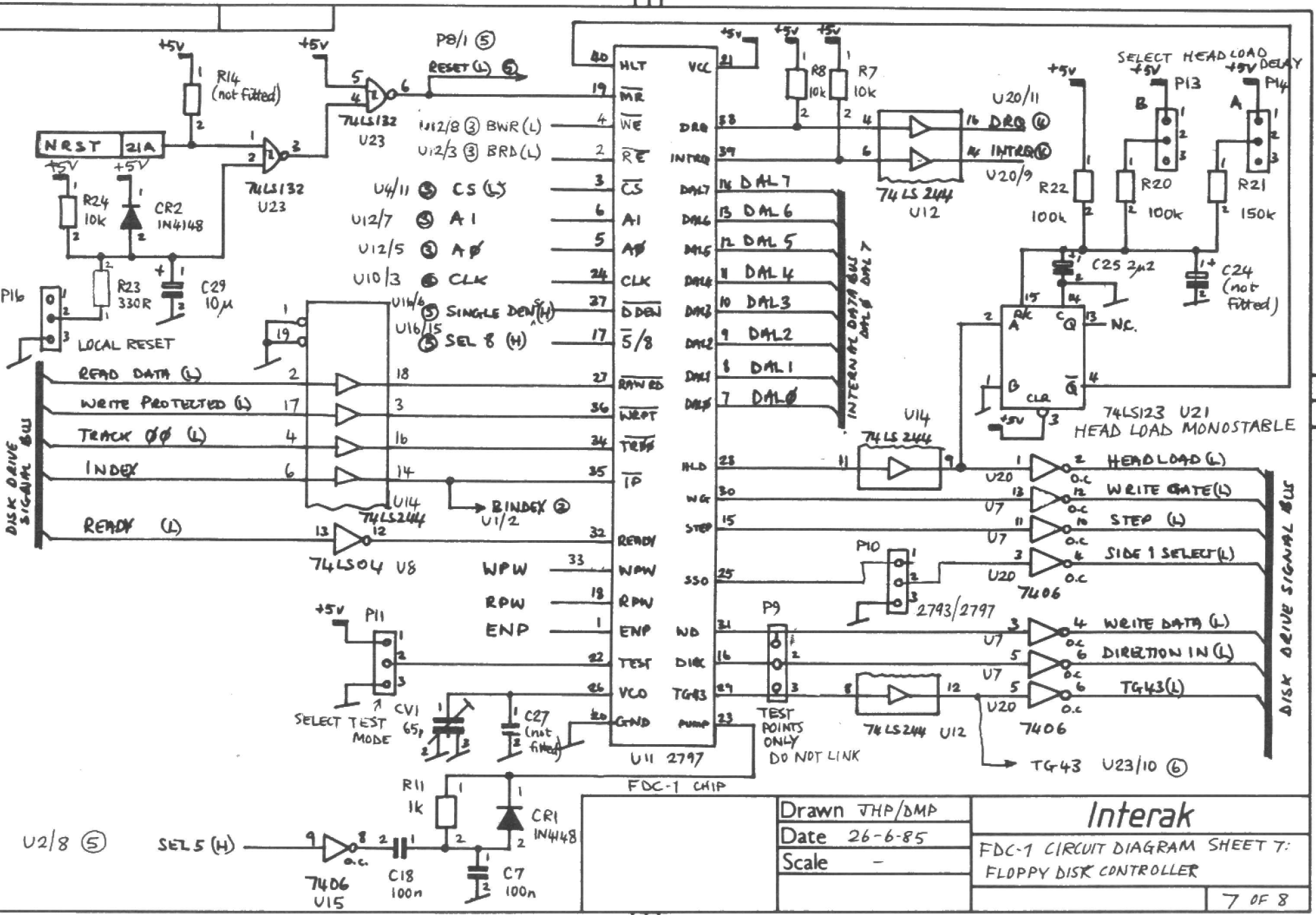
FDC-1 CIRCUIT DIAGRAM SHEET 5:
LATCH & DRIVE SELECT

5 OF 8

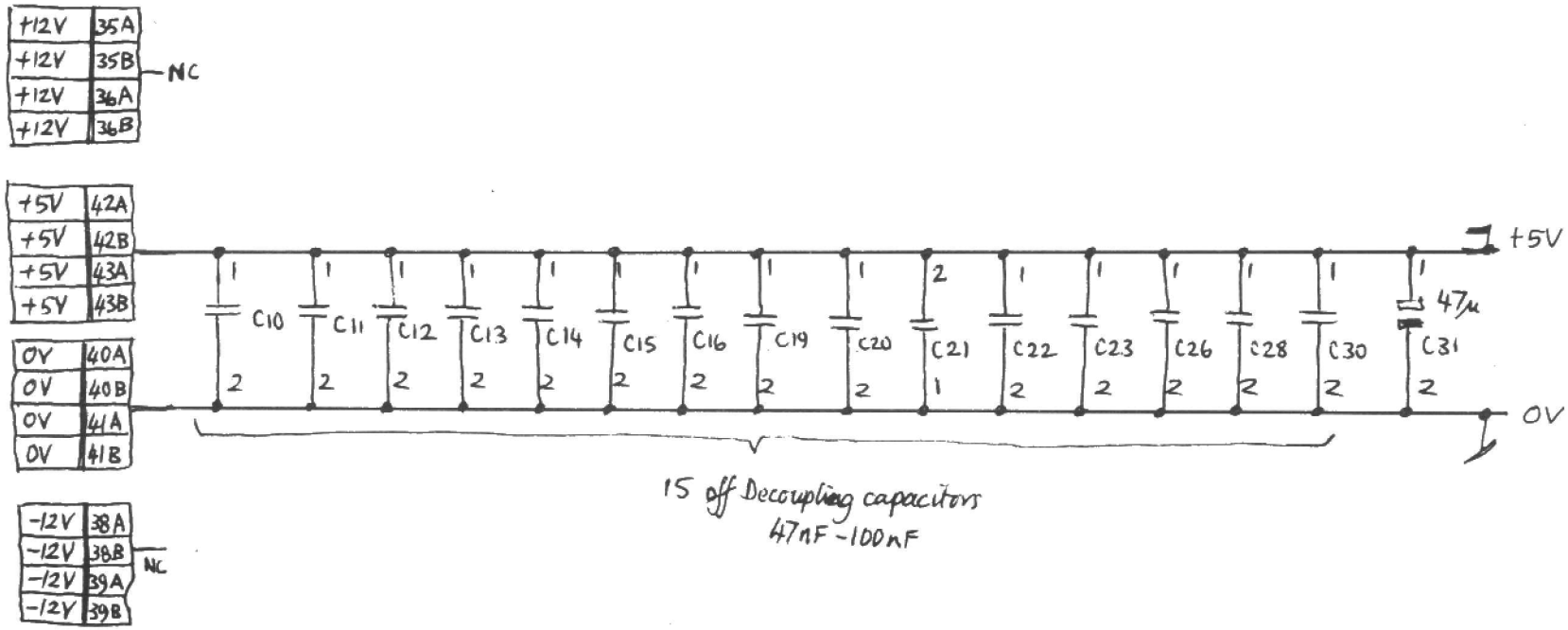


	Drawn JHP/DMP	Interak
	Date 26/6/85	FDC-1 CIRCUIT DIAGRAM SHEET 6 PRECOMPENSATION AND 5/8 SWITCHING
	Scale –	6 OF 8

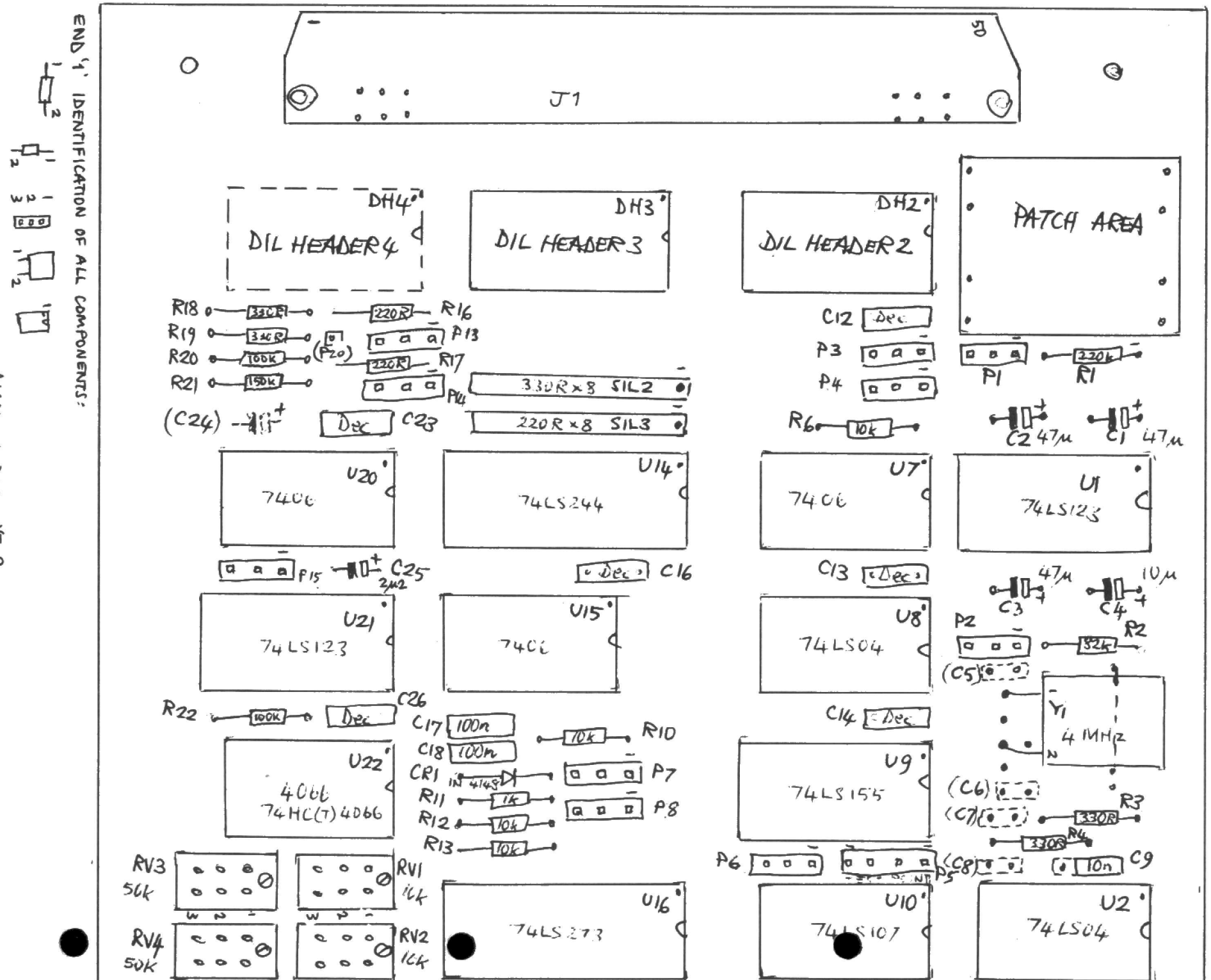
PAGE X5-6


NRST
21A
R14 (not fitted)
R24 10k
CR2 IN4148
R23 330R
C29 10µ
P16
LOCAL RESET
74LS132 U23
P8/1 ⑤
RESET (L) ⑤
U12/8 ③ BWR (L)
U12/3 ③ BRD (L)
U4/11 ⑤ CS (L)
U12/7 ⑤ A1
U12/5 ⑤ A0
U10/3 ⑥ CLK
U16/4 ⑤ SINGLE DEN (H)
U16/15 ⑤ SEL 8 (H)
READ DATA (L)
WRITE PROTECTED (L)
TRACK 00 (L)
INDEX
READY (L)
DISK DRIVE SIGNAL BUS
74LS244 U14
74LS04 U8
BINDEX ⑥ U1/2
WPW
RPW
ENP
U11 2797
FDC-1 CHIP
HLT
MR
WE
RE
CS
A1
A0
CLK
DDEN
5/8
RAWRD
WRPT
TEST
IP
READY
WPW
RPW
ENP
TEST
VCO
GND
VCC
DRQ
INTRQ
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
HLD
WG
STEP
SSO
WD
DIRC
TG43
PUMP
INTERNAL DATA BUS DAL 7
R8 10k
R7 10k
74 LS 244 U12
U20/11 DRQ ⑭
U20/9 INTRQ ⑫
SELECT HEAD LOAD DELAY
P13
P14
R22 100k
R20 100k
R21 150k
C25 2µ2
C24 (not fitted)
74LS123 U21
HEAD LOAD MONOSTABLE
NC.
U14 74 LS 244
HEAD LOAD (L)
WRITE GATE (L)
STEP (L)
SIDE 1 SELECT (L)
WRITE DATA (L)
DIRECTION IN (L)
TG43 (L)
7406
U20
U7
P10
2793/2797
P9
TEST POINTS ONLY DO NOT LINK
74 LS 244 U12
TG43 U23/10 ⑥
P11
SELECT TEST MODE
CV1 65p
C27 (not fitted)
R11 1k
CR1 IN4148
U2/8 ⑤
SEL 5 (H)
7406 U15
C18 100n
C7 100n
Drawn JHP/DMP
Date 26-6-85
Scale –
Interak
FDC-1 CIRCUIT DIAGRAM SHEET 7: FLOPPY DISK CONTROLLER
7 OF 8

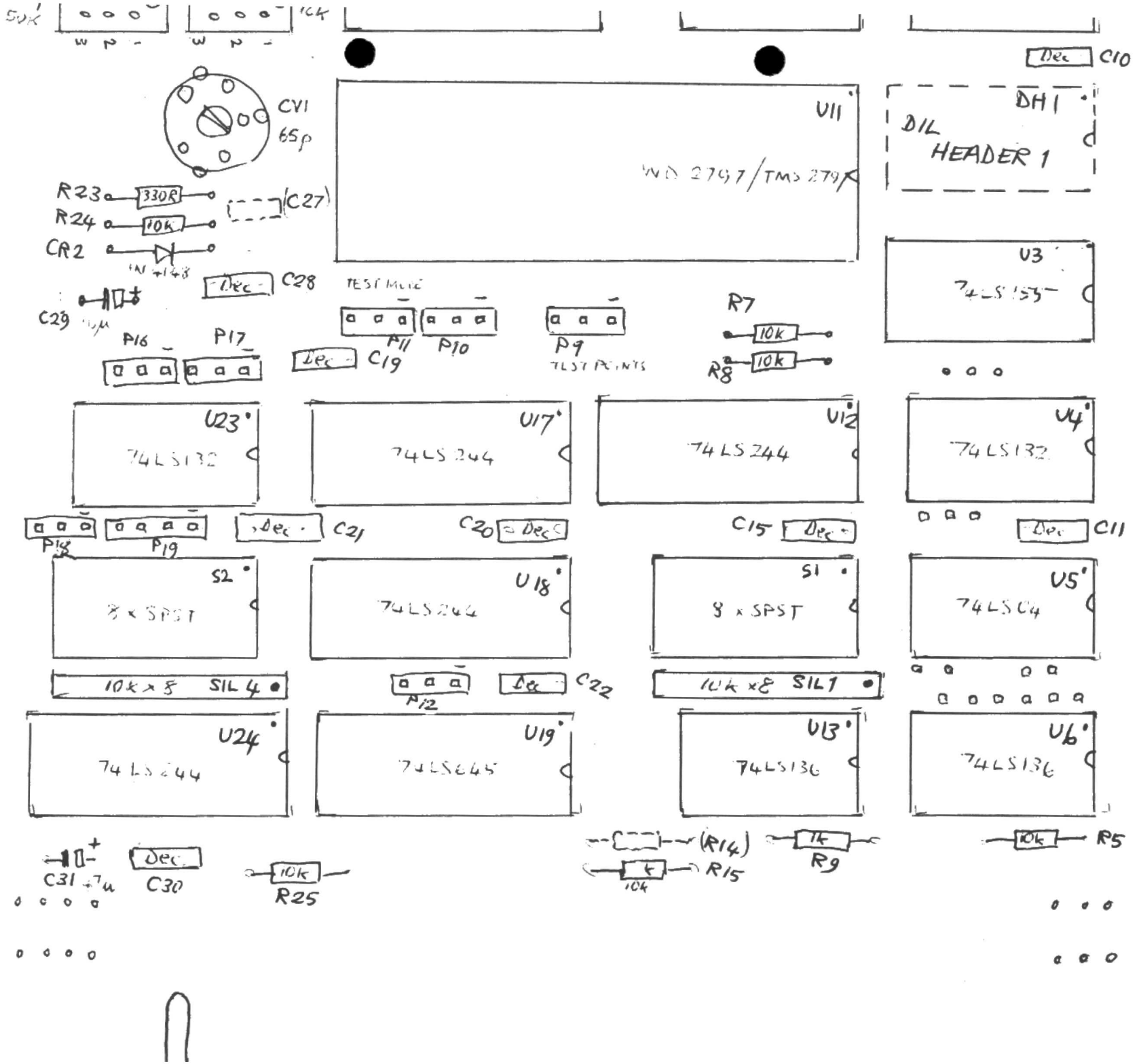
PAGE X5-8



	Drawn DMP	**Greenbank Electronics**
	Date 26-6-85	FDC-1 CIRCUIT DIAGRAM SHEET 8: DECOUPLING CAPACITORS, POWER SUPPLIES
	Scale –	8 OF 8



END '1' IDENTIFICATION OF ALL COMPONENTS:


50K
104
Dec C10
DH1
DIL HEADER 1
CV1
65p
U11
WD 2797/TMS 279X
R23 330R
R24 10K
(C27)
CR2
IN 4148
Dec C28
C29 10µ
TEST MODE
P11
P10
P9
TEST POINTS
R7 10k
R8 10k
U3
74LS153
P16
P17
Dec C19
U23
74LS132
U17
74LS244
U12
74LS244
U4
74LS132
P18
P19
Dec C21
C20 Dec
C15 Dec
Dec C11
S2
8 x SPST
U18
74LS244
S1
8 x SPST
U5
74LS04
10k x 5 SIL 4
P12
Dec C22
10k x 8 SIL 1
U24
74LS244
U19
74LS645
U13
74LS136
U6
74LS136
C31 +7u
Dec C30
10k R25
(R14)
R15
104
R9
10k R5

COMPONENT PARTS LIST FOR FDC-1 CARD

Issue X1 Date: July 1985

LISTED BY COMPONENT REFERENCE NUMBER

Resistors 0.25W (0.4" pitch)

R1	220k	0.4"	R14	-	0.4"
R2	82k	0.4"	R15	10k	0.4"
R3	330R	0.4"	R16	220R	0.4"
R4	330R	0.4"	R17	220R	0.4"
R5	10k	0.4"	R18	330R	0.4"
R6	10k	0.4"	R19	330R	0.4"
R7	10k	0.4"	R20	100k	0.4"
R8	10k	0.4"	R21	150k	0.4"
R9	10k	0.4"	R22	100k	0.4"
R10	10k	0.4"	R23	330R	0.4"
R11	1k	0.4"	R24	10k	0.4"
R12	10k	0.4"	R25	10k	0.4"
R13	10k	0.4"			

SIL Resistors (Use Sockets)

SIL1 9-pin 8x10k	SIL3 9-pin 8x220R
SIL2 9-pin 8x330R	SIL4 9-pin 8x10k

Variable Resistors (Multi, Square Type)

RV1	10k	RV3	50k
RV2	10k	RV4	50k

Capacitors

C1	47u Al	0.2"	C17	100n Py	0.2"
C2	47u Al	0.2"	C18	100n Py	0.2"
C3	47u Al	0.2"	C19	Dec	0.2"
C4	10u Al	0.2"	C20	Dec	0.2"
C5	-	0.1"	C21	Dec	0.2"
C6	-	0.1"	C22	Dec	0.2"
C7	-	0.1"	C23	Dec	0.2"
C8	-	0.1"	C24	-	0.2"
C9	10n Cer	0.1"	C25	2u2 Al	0.2"
C10	Dec	0.2"	C26	Dec	0.2"
C11	Dec	0.2"	C27	-	0.2"
C12	Dec	0.2"	C28	Dec	0.2"
C13	Dec	0.2"	C29	10u Al	0.2"
C14	Dec	0.2"	C30	Dec	0.2"
C15	Dec	0.2"	C31	47u Al	0.2"
C16	Dec	0.2"	CV1	65p Trim	

Diodes

CR1	1N4148	0.4"	CR2	1N4148	0.4"

LISTED BY COMPONENT VALUE

Resistors 0.25W (0.4" pitch)

220R	2	R16,17	(0.4")
330R	5	R3,4,18, 19,23	(0.4")
1k	2	R9,11	(0.4")
10k	10	R5-8,10,12,13 15,24,25	(0.4")
82k	1	R2	(0.4")
100k	2	R20,22	(0.4")
150k	1	R21	(0.4")
220k	1	R1	(0.4")
-	1	R14	(0.4")

("-" = not used)

SIL Resistors (Use Sockets)

9-pin 8x220R	SIL3
9-pin 8x330R	SIL2
9-pin 8x10k	SIL1,4

Variable Resistors (Multi, Square Type)

10k	1	RV1,2
50k	2	RV3,4

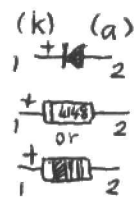
Capacitors

65p Trim	1	CV1
10n Cer	1	C9
Dec	15	C10-16,19-23, 26,28,30
100n Poly	2	C17,18
2u2 Al 20%	1	C25
10u Al 20%	2	C4,29
47u Al 20%	4	C1,2,3,31
-	6	C5-8,24,27

"Cer" = Ceramic
"Dec" = 47-100n Decoupling grade polyester, or Ceramic
"Al" = Low Leakage Min. Aluminium
"-" = None fitted

Diodes

1N4148	2	CR1,2 (0.4")



COMPONENT PARTS LIST FOR FDC-1 CARD (continued)

Quartz Crystal (0.2" Pitch)

Y1	4.0 MHz

Integrated Circuits (Use Sockets)

U1	74LS123	(16)	U13	74LS136	(14)
U2	74LS04	(14)	U14	74LS244	(20)
U3	74LS155	(16)	U15	7406/16	(14)
U4	74LS132	(14)	U16	74LS273	(20)
U5	74LS04	(14)	U17	74LS244	(20)
U6	74LS136	(14)	U18	74LS244	(20)
U7	7406/16	(14)	U19	74LS645	(20)
U8	74LS04	(14)	U20	7406/16	(14)
U9	74LS155	(16)	U21	74LS123	(16)
U10	74LS107	(14)	U22	4066	(14)
U11	2797	(40)	U23	74LS132	(14)
U12	74LS244	(20)	U24	74LS244	(20)

DIL Switches (Use Sockets)

S1	16-pin 8xSPST
S2	16-pin 8xSPST

0.1" Pitch Pin Assemblies

P1	3-pin	P11	3-pin
P2	3-pin	P12	3-pin
P3	3-pin	P13	3-pin
P4	3-pin	P14	3-pin
P5	5-pin	P15	3-pin
P6	3-pin	P16	3-pin
P7	3-pin	P17	3-pin
P8	3-pin	P18	4-pin
P9	3-pin	P19	3-pin
P10	3-pin	P20	-

DIL & SIL Sockets

9-pin SIL	2	SIL1,2,3,4
14-pin DIL	12	U2,4,5,6,7,8,10,13,14,20,22,23
16-pin DIL	8	DH2,3; S1,2; U1,3,9,21
20-pin DIL	7	U12,14,16,17,18,19,24
40-pin DIL	1	U11
not used	2	DH1,4

Sundry

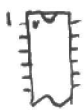
16-pin DIL Header (use 16-pin sockets)	DH1,4	2
JLink JL1-4,6-8,10-14,16-19		16
Not used	DH2,3	2

Quartz Crystal (0.2" Pitch)

4.0 MHz	1	Y1

Integrated Circuits (Use Sockets)

2797	1	U11	(40 pin)
4066/74HC	1	U14	(14 pin)
7406/16	3	U7,5,20	(14 pin)
74LS04	3	U2,5,8	(14 pin)
74LS107	1	U10	(14 pin)
74LS123	2	U1,21	(16 pin)
74LS132	2	U4,23	(14 pin)
74LS136	2	U6,13	(14 pin)
74LS155	2	U3,9	(16 pin)
74LS244	5	U12,14,17 18,24	(20 pin)
74LS273	1	U16	(20 pin)
74LS645	1	U19	(20 pin)



DIL Switches (Use Sockets)

16-pin 8xSPST	2	S1,2

0.1" Pitch Pin Assemblies

3 pin	17	P1-4,6-17,19
4 pin	2	P5,18
-	1	P20

"-" = None fitted

COMPONENT PARTS LIST FOR FDC-1 CARD (continued)

OPTIONS

Note Options: The items marked "" in the parts lists are not supplied in the standard kit of parts for the FDC-1; however they are available separately, as indeed are all the components.

PCB and Manual
*FDC-1 p.c.b, sold separately as "FDC-1 Bare Board"
*Manual, sold separately as "FDC-1 User's Manual" Note! not available yet
*Manual, sold separately as "FDC-1 Software Manual" Note! not available yet

Card Front
*1 off Kit (1 inch wide) including fixings and mounting brackets, new type or old (RS) type, according to type of rack used.

Software

*Boot EPROMS for CPU card
*Formatter disk (for certain EPROMs only)
*CP/M 2.2 on Disk
*BIOS alone

Cables and connectors

*Ribbon cable header J1 pcb mounting (to mount on card)
ditto J1' panel mounting (to mount on front panel)

*Pin assembly kit, wire-wrapping wires for panel mounting
*30 prestripped wires 38 mm (signal)
*30 prestripped wires 48 mm (ground)
*20 5-way 0.1" pitch pin assemblies

*Interface Cable 1.5m 34 way with connectors for 2 x 3.5" drives
*Interface Cable 1.5m 34 way with connectors for 2 x 5.25" drives
*Interface Cable 1.5m 50 way with connectors for 2 x 8" drives

*Ribbon Cable 34 way, 50 way per metre
*IDC socket (female): 34 way (for 3.5") 50 way (for J1)
*0.1" pcb IDC socket: 34 way (for 5.25") 50 way (for 8")

Resistor Colour Code (Ignore last band (generally gold))

220R	Red, Red, Brown
330R	Orange, Orange, Brown
1k	Brown, Black, Red
10k	Brown, Black, Orange
82k	Grey, Red, Orange
100k	Brown, Black, Yellow
150k	Brown, Green, Yellow
220k	Red, Red, Yellow